Medusa Labs Training

Fibre Channel over Ethernet (FCoE) Protocol (ML245_40G.2014.10)

Investigate the inner workings of FCoE protocol, the newest high-speed storage area networking (SAN) technology.

Get concrete, detailed answers to your questions:

- What features must Ethernet support to deliver fibre channel?
- How is flow control handled?
- How is fibre channel login affected?
- How does a node find a switch?

Learn the answers to these questions and more in comprehensive FCoE Protocol training. Our class is based on the proposed for ratification FCoE standard (FC-BB-6) and the latest real-world test findings based on our testing services. And, each protocol class includes lab time.

Our classes are for test engineers, design engineers, technical product/field support, and SAN administrators who address low-level protocol issues.

Medusa Labs Testing and Training

Viavi Solutions is a leading provider of testing and training services through its Medusa Labs offering that focuses on server, storage, and networking interfaces and protocols. Our engineers and trainers are experts in SAS, SCSI, RAID, iSCSI, SATA, SAS, and FCoE.

Our engineers helped develop some of the industry's key technologies and continue to have a vigorous passion for improving products and sharing their knowledge. This experience and enthusiasm translates into the highest quality testing and training services possible.

We further set ourselves apart by bringing the lab to the classroom through the use of Viavi Xgig® analyzers in every class.

3 Day Course Outline

- Fundamental Elements of FCoE
- Ethernet Review
- Fibre Channel Review
- FCoE Architecture
- DCB Architecture
- FCoE Initialization Protocol
- Trace Analysis
- SCSI Fundamentals

What to Expect

- Never pay extra to view trace captures
- Insight into the standard based on our real-world testing experience
- Instruction from experts with more than 20 years of experience in SAN

Fundamental Elements of FCoE

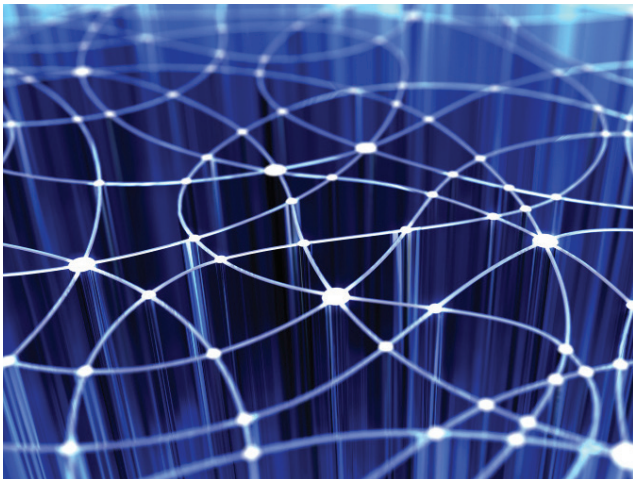
This section identifies the basic features of and the premises upon which FCoE is being designed. FCoE-specific objects and terminology are defined. Upon completion, students can:

- Identify the basic features of FCoE
- Draw a comparison between FCoE and other LAN-based SAN options
- Identify the factors supporting the creation and promotion of FCoE
- Describe the basic concept of FC frame encapsulation
- Identify key design challenges to FCoE
- Understand data center bridging (DCB)

Ethernet Review

This section reviews the basics of the Ethernet protocol with specific emphasis on this technology as the assigned physical and link layer for FCoE. Upon completion, students can:

- Identify the stack that makes up the Ethernet MAC layer
- Explain delivery of 10 G Ethernet
- Identify how Ethernet performs discovery and error recovery
- Identify the parts of the Ethernet header, including the VLAN Qtag
- Define lossless Ethernet



Fibre Channel Review

This section reviews the fundamental concepts related to the FC-2, FC-3, and FC-4 layers of the fibre channel (FC) network stack and identifies FC-specific objects and terminology. Upon completion, students can:

- Define the roles of the port types in FC
- Describe the contents and format of a FC frame
- Identify the steps involved in logging in with a FC switch
- List the features of Class 3 FC
- Describe how FC implements flow control
- Define NPIV and explain how it affects the login process
- Describe the concept of exchange management

FCoE Architecture

This section discusses the architectural concepts and terminology associated with FCoE and discusses both agreed-upon and proposed features. Trace analysis is used to investigate the completion of SCSI input/output (IO) through FC and through FCoE. Upon completion, students can:

- Describe FCoE features and terminology
- Define NPIV
- Define the role of the FCoE forwarder (FCF) and its associated port types
- Define the role of the ENode and identify its associated port types
- Identify the encapsulation frame layout for FCoE frames

DCB Architecture

This section discusses the architectural concepts and terminology associated with DCB. Discusses both agreed-upon features and proposed features. Trace analysis is used to investigate the communication, synchronization, and formatting of these features. Upon completion, students can:

- Describe DCB features and terminology
- Describe the LLDP interaction that facilitates DCB
- List the features encompassed by DCB, such as PFC, CN, and ETS
- Identify and interpret the sections of a DCB exchange (DCBx)
- Define the current state of associated protocols within the industry

FCoE Initialization Protocol

This section details the FCoE Initialization Protocol (FIP) processes and frame format. Trace analysis is used to investigate both the FIP advertisement functions as well as discovery. Upon completion, students can:

- Explain the need for FIP
- Explain the various proposed uses for FIP
- Describe the process by which a node would find a switch using FIP
- Describe the FIP's role in FLOGI
- Describe the FIP's role with Extended Link Services
- Explain how FIP is used to fulfill the "keep alive" requirement

Trace Analysis

This section explores the process and tools needed for taking and interpreting a protocol-level analyzer trace. Upon completion, students can:

- Open a previously captured trace
- Efficiently filter and navigate through the information contained in a trace
- Decipher the interactions between different devices spanning multiple protocols
- Know how an analyzer works
- Know what an analyzer captures and what files are created

SCSI Fundamentals

This section explores basic SCSI concepts. Upon completion, students can:

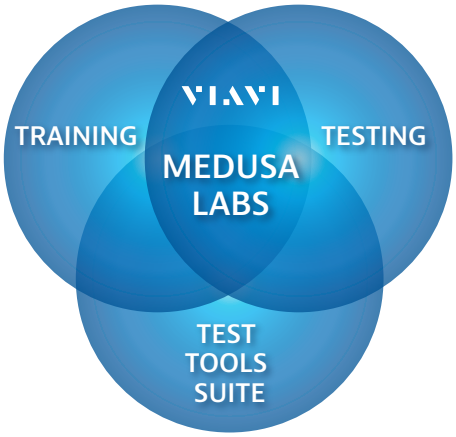
- Define initiator and target roles
- Describe how SCSI exchanges are tracked
- Define read and write workflows
- Define relevant frames for each phase

Xgig Analyzers

We were the first to recognize the importance of using test analysis equipment in the classroom. Today we insist that not only the instructor but also the students use analyzer software during class. No better method exists for reinforcing concepts discussed in a lecture than by "seeing" them in a trace capture. Using the Viavi Xgig analyzer, we show how the protocol works. Whether onsite at your location or at one of our own facilities, every core training course includes lab time.

Medusa Labs Testing Services

We test customers' products quickly and thoroughly in an enterprise environment to ensure that products will survive the rigorous demands of mission-critical applications. Customers come to us for our fast turnaround, superior analysis, excellent results, competitive prices, and, of course, 100% confidentiality. We work hand-in-hand with our customers' engineers to provide solutions along with information. We provide not only the results of our tests, but also the debug, analysis, and regression tests that are needed to ensure that the products we test perform as expected—for your customers.



Medusa Labs Test Tool Suite

Viavi brings years of hands-on expertise and knowledge in the test and validation arena and puts it directly into its Medusa Labs Test Tool Suite, which finds elusive data corruptions, I/O timeouts, I/O loss, system lockup scenarios, and data integrity susceptibility. The tools are rich in debug and logging information to allow for rapid analysis of any found issues. They are designed to stress hardware and signal integrity and function on Linux, Solaris, and Windows so that familiarity on one platform leads to familiarity on all others. The suite was designed specifically for engineers who work with DVT, validation, bring-up, design validation, and quality assurance.

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