Understanding Ethernet and Fibre Channel Standard-Based Test Patterns

An explanation of IEEE 802.3 and NCITS standard test patterns

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Overview

The IEEE 802.3 standards for 1 Gigabit (1G) Ethernet and 10 Gigabit (10G) Ethernet describe several patterns that should be generated for OSI layer 1 and layer 2 testing of components, circuit packs, and even some Ethernet point-to-point circuits. The NCITS standard describes similar patterns for FC-0 through FC-2 layer testing of 1 Gigabit (1G) and 2 Gigabit (2G) Fibre Channel devices.

OSI Model

In order to better understand physical layer testing, the overall Ethernet OSI model must be considered.

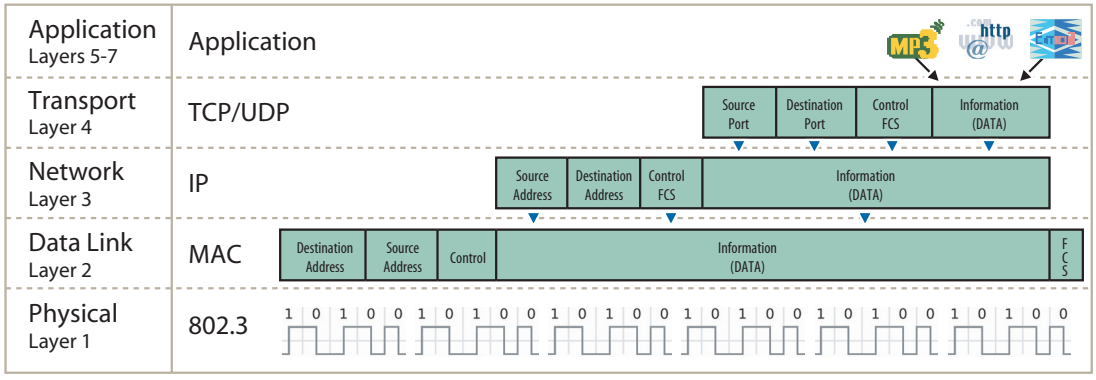

Figure 1. Ethernet OSI model

Figure 1 shows that the addressing for an Ethernet data stream is located in layer 2 and the IP addressing is located in layer 3. The physical layer consists of the bit stream defined by the relevant 802.3 standard.

Fibre Channel follows a very similar organizational structure to Ethernet for the purposes of physical layer testing. The model for Fibre Channel compared to the OSI model is shown in Table 1.

OSI Model	Fibre Channel
Layer 2: Data Link	FC-2
Layer 1: Physical	FC-1
	FC-0

Table 1. Fibre Channel and the OSI model

FC-0 and FC-1 are similar to the physical layer of the OSI model. Fibre Channel's physical layer adds basic flow control functionality and set ordering.

FC-2 is similar to the MAC functionality. In FC-2, Fibre Channel frames are defined, addressed, and a cyclical redundancy check (CRC) is inserted.

For Ethernet, there are three different types of physical layer BER patterns: layer 1 unframed, layer 1 physical coding sub-layer (PCS) synchronized, and layer 2 compliant. In order to understand the differences between the pattern types, the first two layers of the OSI model must be re-examined with more detail, showing the data link and physical layers and their IEEE sub-layers (Table 2).

OSI Layer	IEEE Sub-layer
Layer 2: Data Link	Logical Link Control
	MAC Control
	MAC
Layer 1: Physical	Reconciliation
	xMII
	PCS
	PMA
	MDI
	Medium

Table 2. Expanded OSI model showing the layer 1 and layer 2 sub-layers

Physical Layer

The following section contains a brief description of each sub-layer of the physical layer.

Medium

The medium is the physical medium carrying the data, either fiber or copper.

MDI

The media dependant interface (MDI) is the cable connector between the signal transceivers and the link.

PMA

The physical medium attachment (PMA) contains the transceiver as well as the clock recovery logic for the received data stream.

PCS

The physical coding sub-layer (PCS) provides the logic for encoding, multiplexing, and synchronization of the outgoing symbol stream as well as symbol code alignment, demultiplexing, and decoding of the incoming data stream. The two most commonly used PCS types are 8B/10B for 1G Ethernet, 1G Fibre Channel, and 2G Fibre Channel and 64B/66B for 10G Ethernet LAN and WAN.

xMII

The media independent interfaces, GMII for 1G Ethernet and XGMII for 10G Ethernet, are the separate transmit and receive data paths.

Reconciliation

This sub-layer acts as a command translator and converts MAC layer information to the electrical format required by the layers below it.

Data Link Layer

The combination of the MAC, MAC control, and logical link control (LLC) layers forms the data link layer for Ethernet. The data link layer uses the basic Ethernet frame format, including MAC addressing, MAC control information, and MAC client data, which is often an IP packet.

L1 Unframed, L1 PCS Synchronized, and L2 Compliant Patterns

The pattern descriptions below discuss the three different types of patterns, as defined by the standards, and where they apply within the OSI model.

L1 Unframed Patterns

A layer 1 unframed pattern is a basic bit stream at the appropriate bit rate for the interface – 1.25 Gb/s for Ethernet, 1.063 Gb/s for 1G Fibre Channel, 2.126 Gb/s for 2G Fibre Channel, or 10.313 Gb/s for 10G Ethernet LAN. The PCS coding is not included in this type of BER pattern.

Any circuit card or element, which requires that the pattern pass through the PCS layer, will not allow L1 unframed test patterns to pass through it. The L1 unframed pattern is most often used to test optics or data paths within a circuit pack. It is not passed through any chipset or FPGA that is expecting a valid Ethernet data stream. It is rarely passed through an entire Ethernet circuit pack or a point-to-point Ethernet circuit.

L1 PCS Synchronized Patterns

LAN PHY/Fibre Channel

Layer 1 PCS synchronized signals include the PCS layer as part of the BER pattern. These patterns are formatted using the appropriate 8B/10B symbol format for 1G Ethernet and 1G/2G Fibre Channel or a 64B/66B symbol format for 10G Ethernet LAN. L1 PCS synchronized patterns are passed by any circuit pack or element that requires basic synchronization messages in order to pass traffic.

For 1G Ethernet and 1G/2G Fibre Channel, the L1 PCS synchronized patterns are defined using the correct 10B symbol. The pattern is not created as an 8 bit (8B) symbol and then converted to the correct 10 bit (10B) symbol. Therefore, similar to L1 unframed patterns, L1 PCS synchronized patterns can be analyzed at the bit level.

WAN PHY

For 10G Ethernet WAN, an L1 PCS synchronized pattern is a BER pattern in a SONET/SDH frame with the correct 64B/66B coded pattern inside the SONET/SDH frame. Almost all circuit packs and elements with a 10G Ethernet WAN interface require that the BER pattern be incorporated into a valid SONET/SDH frame.

L1 PCS synchronized traffic passes through any circuit that has no termination or intermediate elements requiring valid layer 2 addressing or CRC values.

L2 Compliant Patterns

Layer 2 compliant patterns are designed to resemble an Ethernet or Fibre Channel frame. The pattern is similar to a basic frame through the data link layer, including a start-of-frame delimiter (SFD), cyclical redundancy check (CRC), and end-of-frame delimiter (EFD). The pattern, however, overwrites all other parts of the frame, including MAC addressing and IP addressing. Only the CRC value remains. The pattern must also have a valid preamble, a minimum inter-frame gap, and a valid frame length.

L2 compliant patterns are passed by circuit packs and elements that are looking for a valid Ethernet frame with a CRC. More specifically, the element or circuit pack must not require a definable MAC address, MAC control information, or LLC information – just the SFD, CRC, and EFD. L2 compliant patterns are not passed by elements that require provisioned MAC addressing or control information.

Pattern Summary and Usage Guidelines

Table 3 shows how the different patterns, including L1 unframed, L1 PCS synchronized, and L2 compliant, relate to the OSI model.

OSI Layer	Ethernet Layer	Pattern Type		
Layer 2: Data Link	Logical Link Control			
	MAC Control			
	MAC			
Layer 1: Physical	Reconciliation			
	xMII			
	PCS			
	PMA			
	MDI	L1 Unframed	L1 PCS Synchronized	L2 Compliant
	Medium			

Table 3. OSI model and pattern type comparison

Each type of pattern has specific uses. Table 4 offers guidelines for the testing environments using the patterns discussed above.

Test Type	Pattern Type			
	L1 Unframed	L1 PCS Synchronized	L2 Compliant	NA
Lab Environment				
Component Test	✓	✓		
Circuit Pack Test		✓		
Element SVT		✓	✓	
Service Provider Environment				
Element SVT		✓		
Layer 1 Circuit Turn-up (Transparent)		✓	✓	
Layer 2 Circuit Turn-up (FCS Aware)		✓	✓	
Switched Ethernet Circuit Turn-up				✓
Routed Ethernet Circuit Turn-up				✓

Table 4. Physical layer pattern usage testing environments

802.3 Standard Patterns (1 Gigabit Ethernet)

The 802.3 standard describes several test patterns that can be used for physical layer testing and component conformance. This standard is mostly focused on clock recovery compliance and bit jitter compliance.

Table 5 lists the 802.3 standard physical layer BER patterns for 1 Gigabit Ethernet.

Pattern Name	Description (in HEX)	Layer
High Frequency Test Pattern (HFPAT)	AA…	L1 PCS Synchronized
Low Frequency Test Pattern (LFPAT)	3 E0…	L1 PCS Synchronized
Mixed Frequency Test Pattern (MFPAT)	F AC 14…	L1 PCS Synchronized
Long Continuous Random Test Pattern (LCRPAT)	BE D7 23 47 6B 8F B3 14 5E FB 35 59 (repeated 126 times)	L2 Compliant
Short Continuous Random Test Pattern (SCRPAT)	BE D7 23 47 6B 8F B3 14 5E FB 35 59 (repeated 29 times)	L2 Complaint

Table 5. 802.3 physical layer Gigabit Ethernet BER patterns

802.3 Gigabit Ethernet Pattern Descriptions

High Frequency Test Pattern

This pattern is designed to test high frequency random jitter (RJ) at a BER of 10^{-12} and the asymmetry of the transition times.

Low Frequency Test Pattern

This pattern is designed to test low frequency random jitter and PLL tracking error.

Mixed Frequency Test Pattern

This pattern is designed to test both random jitter and deterministic jitter (DJ).

Continuous Random Test Patterns

There is both a short (384 bytes) and a long (1512 bytes) continuous random test pattern. Both of the continuous random test patterns are designed to provide broad spectral content and minimal peaking, allowing for the measurement of jitter at either the component or system level.

As shown in Table 5, both the short and long continuous random data patterns are L2 compliant and, therefore, include an SFD, CRC, and EFD.

Since these patterns are layer 2 compliant, they have a MAC address and control information. These values, however, are defined by the test pattern and are not editable.

MAC Destination: BE D7 23 47 6B 8F

MAC Source: B3 14 5E FB 35 39

Type/Length: BE D7

NCITS Standard Patterns (1 and 2 Gigabit Fibre Channel)

The NCITS Fibre Channel standard uses several patterns for physical layer testing (Table 6).

Pattern Name	Description (in HEX)	Layer
Random Data Pattern (RPAT)	3EB0 5C67 85D3 172C A856 D84B B6A6 65	L1 PCS Synchronized
Compliant Random Data Pattern (CRPAT)	Similar to RPAT with SFD, CRC, and EFD	L2 Compliant
Jitter Tolerance Pattern (JPAT)	871E 3871 E3 (repeated >167 times) + AA (repeated >50 times)	L1 PCS Synchronized
Compliant Jitter Tolerance Pattern (CJTPAT)	Similar to JPAT with SFD, CRC, and EFD	L2 Compliant
Supply Noise Data Pattern (SPAT)	ACD4 CACD 4C (repeated 512 times)	L1 PCS Synchronized
Compliant Supply Noise Data Pattern (CSPAT)	Similar to SPAT with SFD, CRC, and EFD	L2 Compliant

Table 6. NCITS physical layer Fibre Channel BER patterns

Each pattern in Table 6 has both a compliant and a non-compliant format. The NCITS standard recommends using the non-compliant version whenever possible. The compliant pattern, although slightly different, offers very similar test functionality and should only be used if the non-compliant format does not work within the testing environment.

NCITS Pattern Descriptions

Random Data Pattern/Compliant Random Data Pattern

These patterns were designed to provide energy across the entire frequency spectrum, and they provide a good basic BER test. These patterns can be thought of as a Fibre Channel PRBS.

Jitter Tolerance Pattern/Compliant Jitter Tolerance Pattern

For receiver jitter tolerance testing, a pattern must expose the receiver's clock data recovery (CDR) to large instantaneous phase jumps. In order to accomplish this, the overall pattern should alternate repeating low transition density patterns with repeating high transition density patterns. This stresses the timing margins in the received eye.

Supply Noise Test Pattern/Compliant Supply Noise Test Pattern

This test sequence represents the worst-case power supply noise introduced by a transceiver.

802.3ae Standard Patterns (10 Gigabit Ethernet LAN and WAN)

The 802.ae standard discusses several patterns that can be used for physical layer testing and component conformance of 10 Gb/s Ethernet cards or circuits (Table 7). Unlike the lower speed Ethernet and Fibre Channel standards, there are no compliant patterns specified in the 802.3ae standard.

Pattern Number	Pattern for 10GBASE-R (LAN PHY)	Pattern for 10GBASE-W (WAN PHY)	Layer
1	B-Seed (B_n, B_i, B_n, B_i)	Mixed Frequency	L1 PCS Synchronized
2	A-Seed (A_n, A_i, A_n, A_i)		L1 PCS Synchronized
3	ITU PRBS-31	ITU PRBS-31	L1 Unframed

Table 7. 802.3ae standard physical layer patterns

LAN PHY Patterns

Understanding patterns 1 and 2 requires an understanding of the basic concept of the seeding process used to create the patterns. Pattern 3 is just a straightforward ITU PRBS-31 pattern.

A-Seed / B-Seed (The Seeding Process)

Patterns 1 and 2 are generated by sending a data pattern into the input of a scrambler function (Figure 2). The data is changed by the scrambler and is placed onto the fiber as the actual bit error rate (BER) pattern. It is important to note that the current equation value, G(x), is based on the previous data output as well as the input data stream.

For pattern 1, the scrambler value G(x) is set to the seed of B_n. The input data is set to a local fault pattern (LF) and traffic is generated for 128 blocks. After 128 blocks, the scrambler equation is reset to seed B_i, the input data pattern is set to an inverted LF pattern, and the process is run for another 128 blocks. This process is then repeated over and over.

For pattern 2, the same process is followed using different seed values and input data. In this case, the input data is set to an all zeros pattern and the seed is A_n for the first 128 blocks. For the second 128 blocks of data, the seed is set to A_i with an all ones pattern for the input data.

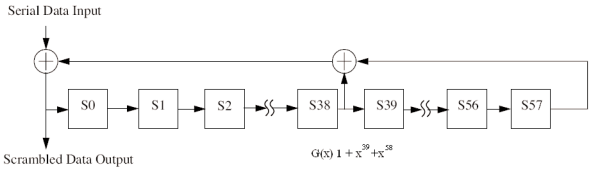

Figure 2. The scrambling process for LAN PHY patterns 1 and 2

Pattern 1 represents typically scrambled data while pattern 2 represents a less typical pattern that can happen by chance.

Table 8 defines the specific scrambler seeds for patterns 1 and 2.

Pattern Segment	Seed (HEX Pattern)
A_n	3C8B 44DC AB68 04F
B_n	3490 6BB8 5A38 884
A_i	(Inverse of A_n)
B_i	(Inverse of B_n)

Table 8. Seed details for the LAN PHY patterns 1 and 2

Therefore, patterns 1 and 2 are the summation of the input signal and the seed.

– Pattern 1: Data pattern = LF, seed = B_n/B_i

– Pattern 2: Data pattern = 0, seed = A_n/A_i

PRBS-31 Pattern

The PRBS-31 pattern does not have the 66B header needed for synchronization. This pattern works well with components that don't require 66B synchronization, but it will most likely put the circuit pack or element under test into a "loss of synchronization" alarm.

The PRBS-31 pattern for LAN PHY is a bit stream running at the 10GBASE-R specification (10.3 Gb/s).

WAN PHY Patterns

The available WAN PHY patterns include a mixed frequency pattern and a PRBS-31 pattern (Table 7).

Mixed Frequency Pattern

The mixed frequency pattern is designed to test the clock recovery circuitry, the WAN interface sublayer (WIS), and the general SONET/SDH performance management overhead.

The mixed frequency pattern is a combination of two patterns being injected into the SONET/SDH frame. First, a standard ITU PRBS-23 pattern is injected into the signal and is processed by the WIS. This component of the mixed frequency pattern verifies WIS operation and allows for the verification of SONET/SDH error monitoring capabilities by injecting standard defects and anomalies.

The second component of the mixed frequency pattern includes the placement of a consecutive identical digit (CID) pattern into the Z0 octet of the SONET/SDH overhead. The CID value, in this case, is an all zero pattern. The Z0 byte is used by the mixed frequency pattern because it is not scrambled by the WIS. This effectively injects a string of zeros into the signal, stressing the clock recovery circuitry.

PRBS-31 Pattern

The PRBS-31 pattern for 10 Gigabit Ethernet WAN PHY is very similar to LAN PHY. There is no SONET/SDH framing/overheard. The pattern runs at the defined bit stream for 10GBASE-W.

10 Gigabit Ethernet LAN and WAN Pattern Testing Functionality

Table 9 lists other tests that can be performed on the network element using the 802.3ae standard patterns for 10 Gigabit Ethernet LAN and WAN. The patterns are defined in Table 7.

Test	Pattern		Corresponding 802.3ae Clause
	LAN	WAN	
Average optical power	1 or 3	MF or PRBS	52.9.3
Extinction ratio	1 or 3	MF or PRBS	52.9.4
Transmit eye	1 or 3	MF or PRBS	52.9.7
Receive upper cutoff frequency	1 or 3	MF or PRBS	52.9.11
Wavelength, spectral width	1 or 3	MF or PRBS	52.9.2
Side mode suppression ratio	1 or 3	MF or PRBS	-
Vertical eye closure penalty calibration	2 or 3	MF or PRBS	52.9.9
Receiver sensitivity	1 or 3	MF or PRBS	52.9.9
Receiver overload	1 or 3	MF or PRBS	-
Stressed receiver conformance	2 or 3	MF or PRBS	52.9.9
Transmitter and dispersion penalty	2 or 3	MF or PRBS	52.9.10
Clock recovery	2	MF	52.9.1
Typical data	1	MF	52.9.1

Table 9. 802.3ae pattern usage including the corresponding 802.3ae clauses

OTN + Ethernet Testing

To date, there is no standard for testing 10 Gigabit Ethernet LAN or WAN within an OTN frame. Most tests are performed by either generating an unframed BER pattern at the actual line rate (10.7 Gb/s for Ethernet WAN or 11.1 Gb/s for Ethernet LAN) or by generating a BER pattern framed inside an OTN frame at the appropriate data rate. It is important to note that generating a standard SONET/SDH client signal inside an OTN signal may not work for WAN PHY testing since there are significant differences in the overhead values between a standard SONET/SDH signal and a 10G Ethernet WAN PHY.

As the testing standard evolves for Ethernet + OTN, this document will be updated accordingly.

RFC2544 Testing

Even after many of the above tests are performed, technicians are often required to prove that the circuit can carry actual Ethernet or Fibre Channel frames with valid OSI layer 2, FC-2, or OSI layer 3 addressing within the defined standard frame sizes. In this instance, RFC2544 is a useful test.

RFC2544 automatically generates different sized frames, including the smallest frame defined by the standard to the largest frame size. It then verifies the maximum throughput per frame size, the round trip latency per frame size, the lost frames per frame size, and the maximum number of back-to-back (minimum frame gap) frames that the environment under test can handle using the appropriate layer 2 (FC-2) or layer 3 addressing.

RFC2544 is defined for layer 2 (Ethernet switch) traffic generation and analysis only. Most test equipment vendors, though, have expanded the test to include layer 3 testing as well as Fibre Channel testing. Although these changes deviate from the standard, RFC2544 provides the technician with one test to cover more than just the basic layer 2 Ethernet switch turn-up test.

Documentation

For more detailed information, refer directly to the IEEE 802.3 or 802.3ae standards for Ethernet or the NCITS-TR-25-1999 standard for Fibre Channel.

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