Testing and Validation of 100G ICs

By Dr. Paul Brooks

Over the past 2 years, a range of 100G products have been developed that leveraged first-generation 100G technology to enable the 100G ecosystem. To align with pricing expectations, port density and feature mix required for mass deployment of 100G has lead to the development of second-generation 100G integrated circuits (ICs).

The 40/100G ecosystem requires three main "types" of digital ICs: physical (phy), Ethernet, and framer/mapper. Of course, many other parts are needed in a 40/100G product; but these digital functions are key to cost-effectively deploying mass product.

Table 1. Three Types of ICs

IC Type	Typical Products	Key Needs
Phy Chips	Gearbox (for 40/100G pluggable optics or CFPs) SERDES (40G serial)	Physical layer validation
Ethernet and Enterprise	Ethernet ports, high port count	Phy and L1-L3 (higher layers achieved via firmware and other methods)
Framer and Mapper	OTN framers and multi-plexers, among others	OTN features as well as phy

Physical Layer

With parallel lane speeds in excess of 10 Gbps, the demands placed on the physical layer by 40/100G jumped significantly over the current 10G products. The challenges are intense for areas such as signal integrity and signal timing, especially over multiple components and connectors. These challenges are compounded by the margin requirements needed for success and cost-effective mass deployment.

One of the key components in 100G is the pluggable optical module. The CFP form factor was used in the first generation and to offer forward compatibility with future 100G technology it uses 10 x 10G electrical but 4 x 25G photonic interfaces (future input/output [I/O] will be at 4 x 25G for both optical and electrical domains). The pluggable optical module must convert the 10 x 10G signal into 4 x25G, which is achieved with a "gearbox" or multiplexer/demultiplexer IC (or IC set). Clearly this high-performance IC inside an optical module will have a significant impact in module power consumption, cost, and volume. First-generation gearboxes may require exotic technology to meet performance requirements; however, modern complementary metal oxide semiconductor (CMOS) processes may allow CMOS gearboxes to offer the lower power and more aggressive price points required for mass deployment.

A new generation of 40G Serializer/Deserializer (SERDES) are also being developed that allow interoperation with legacy 40G serializers but offer a more flexible 4 x 10G interface on the host side. These parts will require validation of the 40G serial side, especially the demanding standards of synchronous optical networks (SONET) (such as for jitter) and the 4 x 10G host side. The Viavi Solutions 40G Jitter test set also offers an optional electrical I/O, which is ideal for IC test and validation.

Ethernet and Enterprise

First-generation 100G products often used the flexibility and performance offered by high-end field-programmable gate arrays (FPGAs), such as the Altera Stratix IV or Xilinix Virtex series, that enable quick 'time to market' especially with the uncertain nature of early standards. (The IEEE standardized 100G via IEEE 802.3ba in June 2010, but companies such as Viavi had been shipping pre-standard 100G products since 2009). While FPGAs offer flexibility and good performance, they do not offer the price and port density needed in mass deployment applications, especially in the Enterprise space. Their flexibility, especially in their fabric, often mean that they cannot offer the feature density and price optimization that dedicated ICs can, as summarized in Table 2.

Table 2. Feature density and price optimization of the two generations of ICs

Generation	Flexibility	Port Density	Price
First	Very important, often pre-standards	Not critical	Not critical, few vendors sell at premium
Second	Post standards, clearly defined features	Critical, often xN ports/IC	Very price sensitive, competitive market

Framers and Mappers

The optical transport network (OTN) offers a wide, flexible range of tributaries and mappings and the flexibility and range of potential (future) configurations often mean that this area is addressed with FPGAs, even at maturity. The development of the Internet Protocol (IP) is the key value in this area.

Test Areas

The test area coverage can be broken down into the four main areas shown in Table 3.

Table 3. Four main areas of test area coverage

Test Area	Key Features
Physical Layer Unframed BERT	Signal integrity validation, conformance to standards (for sensitivity and timing, among others), margin, skew across lanes, and jitter Usually used in conjunction with the tests for the physical layer to show bit error ratio (BER) performance against physical parameters, such as timing, voltage swing, skew, clock jitter, operating voltage, and temperature.
Ethernet Validation and Performance	Framed Ethernet data is used in performance parameters, including measuring and validating basic bit errors through to Ethernet QoS.Validates the response for invalid data and packets. Interworking and performance tests, such as RFC 2544, can be combined with other tests including physical layer.
OTN Compliance and Performance	Validation of OTN compliance, muxing structure, behavior of components, such as mappers, against a range of clients. Checks the variation of client line rates, errors in client, and interaction between clients. Validates FEC performance. Again, all of these tests can be conducted ogether with physical layer tests (or conducted together with Ethernet client traffic).

Ethernet and OTN mapper IC manufacturers often have a very high degree of integration, because it is "expensive" for 40G and 100G (in terms of power and I/O pin count) to move signals on and off IC, so people are driving higher layers of integration. Previously a solution may have been chipset-based on two to three ICs, where now it will likely be one very large IC for 40/100G. Also note that physical layer testing is likely required in every case.

The Viavi ONT 40/100G is unique because it combines the deep physical layer testing features (such as electrical signal control, jitter, and skew) together with comprehensive testing at the Ethernet and OTN layers. Indeed the OTN features are very deep and broad, making them ideal for complete validation of OTN from OTU4 down to ODU0 and ODUflex

ONT test set capable of supporting technology from 51 Mbs to 111.8 Gbs in one unit

The following examples highlight validation of 100G IC functionality using the ONT 100G.

Case 1: CMOS gearbox IC for 100G CFP

Figure 1 shows a typical 100G CFP block diagram.

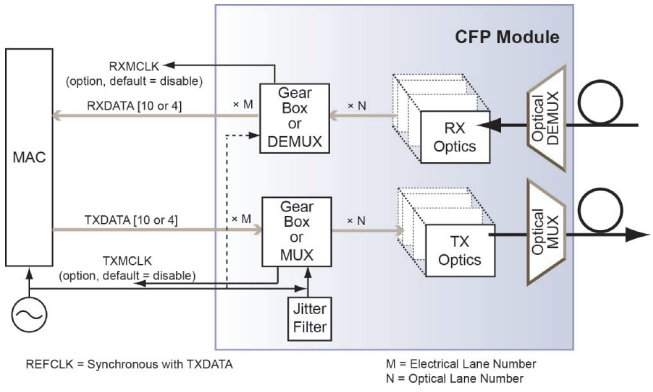

Figure 1. Typical 100G CFP block diagram

One of the key components in diagram is the gearbox (or multiplexer/demultiplexer [MUX/DEMUX]) IC set that provides the 10 x 10G to 4 x 25G conversion. The impact of data timing is critical with parallel high-speed data, clock multipliers, and FIFOs. Because we are testing on the 10G host side, we must first set up a loop on the 25G side,

which can be achieved photonically (if the gearbox is incorporated in a CFP module) or electrically in a test board. The reference clock (normal lane speed /16) is also required by the gearbox for the internal clock multiplier; the ONT can supply a differential reference clock (at either /16 or /64 rates). The ONT can also use the unique Viavi electrical CFP adapter shown in Figure 2 to allow direct interfacing to test and evaluation boards for the gearbox and multiplexer ICs.

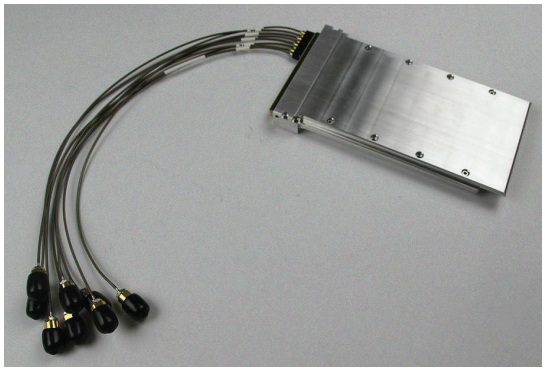

Figure 2. Electrical CFP adapter with partial cable set connected

Typically, we conduct basic pseudorandom bit sequence (PRBS) pattern tests; however, a normal 10 x 10G pattern cannot be used through the gearbox as the 10:4 mux/demux process can reorder the bit pattern in the individual 10G streams, which is why 100GE uses the concept of 20 x 5G virtual lanes. The ONT supports unframed 10 x 2 x 5G mode which allows for sending gearbox transparent PRBS and digital words. Once the gearbox can pass basic traffic, then the parameters may be adjusted, including pre-emphasis and voltage swing, dynamic skewing of the individual data lanes, and clock jitter. The IEEE 802.3ba sets out requirements for performance against parameters, such as skew variation, which can be validated quickly using the ONT. Furthermore, if errors do occur during validation, the applications and fine control of parameters can be used to determine the location of the failure.

Case 2: Ethernet 100G IC

The first-generation 100GE was based on FPGAs that allowed the quick development of pre-standard products developed, but FPGA solutions cannot offer the high density and cost point that Enterprise customers need. Typical switch ICs require 16 x 40GE ports (perhaps 8 x 100GE ports) per IC for the next generation of high-density Enterprise switches, because they must directly interface with a range of pluggable 40/100GE optics from various vendors. They must also support a wide range of Ethernet applications. Validation of the physical interface must be performed to the same levels as those for the phy ICs; however, this is no longer possible with the unframed patterns (such as raw PRBS) used in the first case.

The more complex ICs used in the Ethernet switches require higher layer (Layer 2 and 3) framed signals to complete the internal loopback to perform end-to-end testing. In this case, it is possible to use the ONT to validate the physical layer (such as dynamic skew, pre-emphasis, and clock jitter) while carrying framed Ethernet traffic. Indeed the ONT allows deep stress testing on the physical layer while monitoring the impact on higher Ethernet layers. For example, users can adjust the clock offset to the maximum permissible rate, then add dynamic skew on the physical layer while carrying full rate Ethernet traffic. Users can then ascertain the impact of the clock offset and dynamic skew on Ethernet throughput and QoS, which is not possible with compartmentalized testing.

The ONT supports comprehensive Ethernet testing at Layers 2 and 3 and can set up multiple traffic profiles, manage traffic bandwidth, and manipulate key parameters well beyond normal limits, such as interpacket gap (IPG). Setting the IPG below the normal minimum, coupled with a minimum packet size and extreme limits of clock offset, allows us to view the behavior of the IC under test at the extreme margins of performance, in this case extreme high packet rate. Observing the failure mode under these conditions can help vendors see their parts failing in a controlled and predictable manner. In addition such testing can give clear insight into factors that will impact 'Quality of service' in actual deployment of equipment.

Case 3: Validation of OTN Framer IC

The very flexibility of the OTN allows a wide range of client and tributary configurations that leads to complex implementation needs that may evolve over time; and therefore, FPGA-based designs are often the core of such implementations. The IP for these implementations must be validated against a wide combination of possible clients and tributaries, and the margin conditions (clock rates, error profiles, and tributary types) must also be established. It is important to validate that the framer/mapper implementation behaves in a predictable manner, especially regarding failure mode towards invalid conditions.

The validation of the FEC IP provides a simple example where the ONT offers a comprehensive FEC stress test application that allows for stressing of correctable and uncorrectable errors (both defined in rows and columns). This application allows for full control over all FEC parameters and can fully validate FEC compliance. This FEC test can be run in parallel with a complete OTN traffic structure (for example, ODU0 → ODU1 → ODU2 → ODU4) and while stressing the physical layer (dynamic skew, clock offset, and pre-emphasis). Complete margin testing offers full confidence in IC and IP operation under true worst-case conditions.

Figure 3 shows the ONT FEC stress application running an FEC validation process. It offers comprehensive coverage of FEC validation for all types of correctable and uncorrectable errors that can occur.

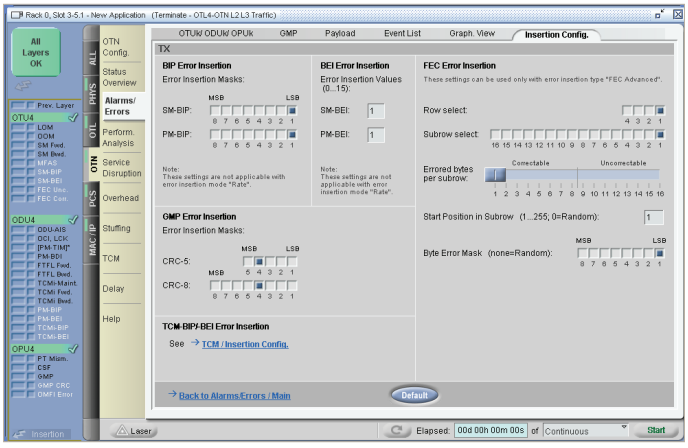

Figure 3. ONT FEC Stress and Validation test screen

Conclusion

Successful and cost-effective deployment of 100G will depend upon reliable components. Complex ICs will be required to carry out a wide range of functions encompassing both physical and protocol layers over parallel fast data buses and extremely high traffic rates. Such demanding complexity coupled with "time to market" needs indicates the criticality for margin testing products under worst-case conditions and testing the physical layer, Ethernet, and OTN in parallel. The ability to stress components well above normal conditions (such as dynamic skew, clock rate, traffic throughput, IPG, and FEC) provides critical information about IC performance margin and failure mode.

Contact Us **+1 844 GO VIAVI**
(+1 844 468 4284)

To reach the Viavi office nearest you,
visit viavisolutions.com/contacts.

testing100gics-wp-lab-tm-ae
30168415 900 0611