G.709 – FEC testing

Guaranteeing correct FEC behavior

Capabilities and Benefits

Techniques in Detail

Example

The ONT-503/506/512 optical network tester from JDSU which delivers in-depth analysis of FEC algorithm implementation as well as analysis of FEC related parameters, has the most comprehensive FEC testing functionality on the market today.

To better understand and apply the advantages enabled through this funtionality, this paper has been prepared to provide in depth information on: the FEC manipulation capability of the ONT-5xx and the implemented FEC test functionality that helps users achieve reduced design and verification times for the development and deployment of FEC systems.

The importance of FEC testing

FEC testing is essential in:

- Verifying correct implementation of the FEC algorithm in FEC encoders and decoders in an R&D environment
- Performing maximum stress testing of network elements (NE) with maximum number of possible errors. This is a requirement for example when performing system verification testing
- Validating correct installation (deployment and integration) of NEs and final installation tests

Implementation of FEC in ITU-T G.709

The G.709 recommendation employs the Reed-Solomon code RS(255/239) which stipulates that 239 bytes be used as information bytes to calculate the FEC parity check of 16 bytes (255-239).

An OTN frame consists of 4 OTU-rows. An OTU-row is split into 16 sub-rows (code words) each consisting of 255 bytes. The sub-rows are formed byte interleaved, which means that the first sub-row contains the first OH byte, the first payload byte and the first FEC byte. The FEC byte of each sub-row is inserted into byte position 240. This is true for all 16 sub-rows. Figure 1 illustrates this process.

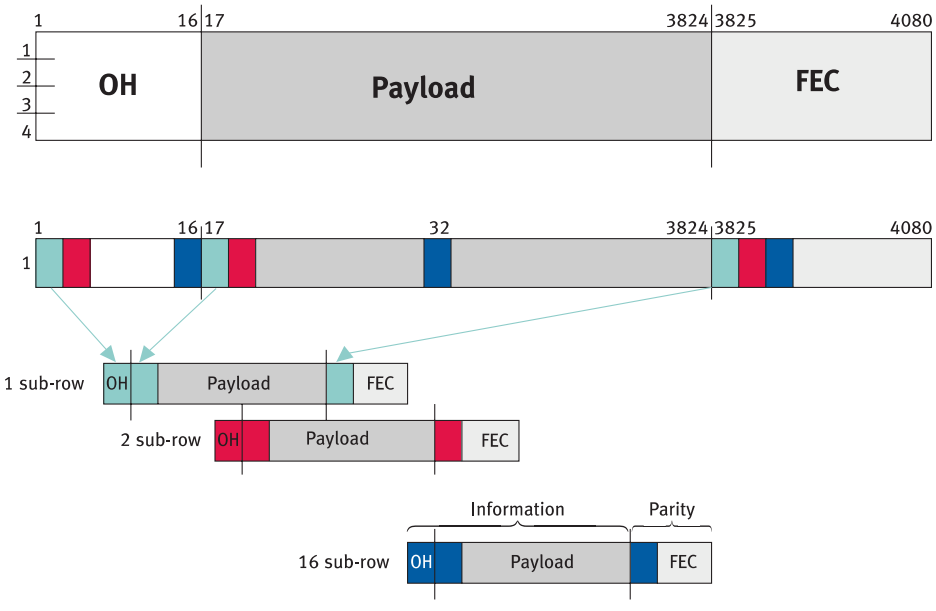

Figure 1: OTN frame

ONT's FEC testing capabilites and their benefits

Pre-defined FEC testing

FEC_corr & FEC_uncorr:

Simple, one-button click, FEC error insertion allows the installer to verify the FEC algorithm in the field.
If failure occurs or improper operation detected in performing this straightforward test, further analysis (FEC_adv) is required.

FEC_max:

A single button click, delivers clear PASS / FAIL criteria of the device under test (DUT).
This maximum stress test inserts the maximum number of possible errors a DUT should still be able to correct entirely in accordance with ITU-T G.709 recommendations.
If failure occurs or improper operation is detected in performing this straightforward test, further analysis (FEC_adv) is required.

User-defined FEC testing

FEC_adv:

This tool allows the user to perform detailed testing on a particular subset of all possible sections of the OTU-frame for errors.

This is required for:

- Verifying FEC encoder and decoder design
- Enabling the user to pinpoint failures or improper operation of the FEC algorithm design. This allows fast detection of poorly designed encoders and decoders used for the encoding/decoding of all 64 sub-rows.

The Reed-Solomon code is capable of detecting 16 byte (symbol) errors or correcting up to 8 byte errors in a sub-row.

In order to explain the various FEC insertion methods the ONT-5xx offers, a matrix is created as illustrated in figure 2.

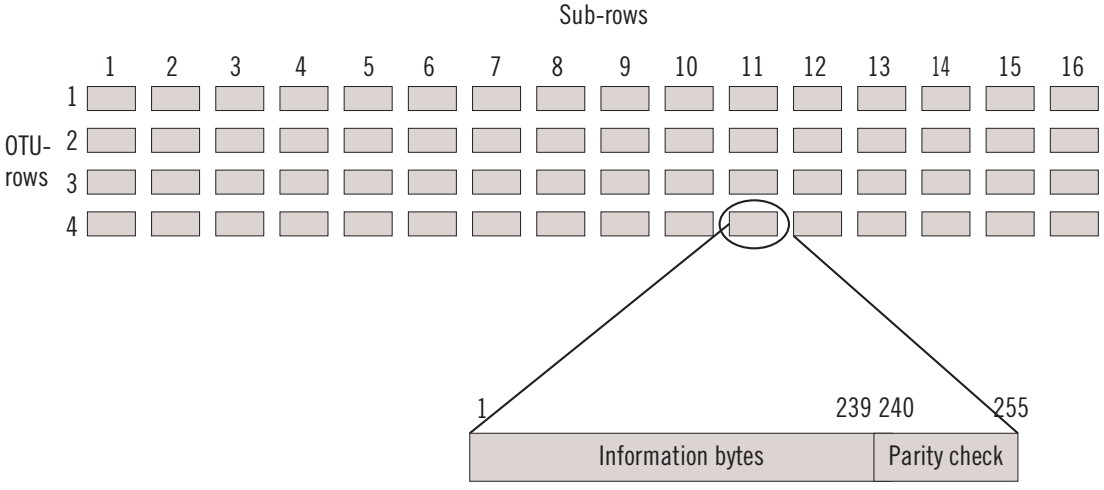

Figure 2: Matrix illustrating the 4 OTU-rows and all 16 sub-rows for each OTU-row.

FEC functionality of the ONT-5xx OTN module

The FEC error generation and detection capability of the ONT can be divided into two significant areas: pre-defined testing of FEC functionality (FEC_correctable, FEC uncorrectable and FEC_maximum), and user-defined (expert) testing (FEC_advanced).

FEC_correctable error insertion

As the error description suggests, when inserting FEC_corr errors, the DUT should still be capable of correcting these errors. This is a simple test used by field engineers in carrying out initial inspections to verify the correct installation of the NEs.

The ONT-5xx therefore displays no error reading as the DUT should correct the inserted FEC error.

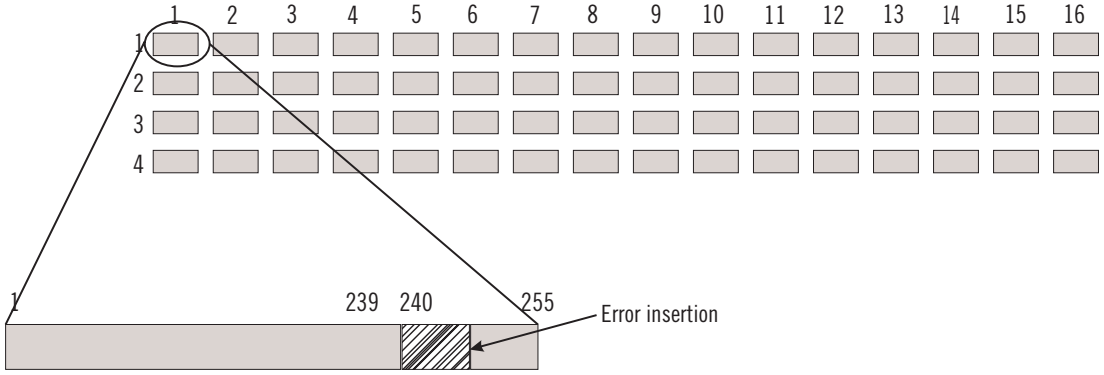

Figure 3: Insertion of errors in the first sub-row of the first OTU-row

The implementation in the ONT is performed by inserting errors in the first sub-row of the first OTU-row as illustrated in the figure 3. Given that the RS code is capable of correcting up to 8 symbol errors in a sub-row, exactly 8 bytes are errored in the dedicated sub-row. The byte inversion is implemented from byte position 240 to 247 of the sub-row shown in the figure 3.

Why insert the errors in the FEC section of the OTU-frame?

The position for the 8 byte inversions is selected on the basis that should the FEC decoder be unable to correct the errors, the original payload can still be made completely available given that the errors are only inserted in the FEC section of the OTU-frame.

Why insert errors in first sub-row of first OTU-row?

Assuming that 16 encoders are used for all OTU-rows in the implementation of FEC, it would be sufficient to test only one encoder in an OTU-row. This is due to the fact that all encoders for the sub-rows should have the same design and should also have been subjected to maximum stress testing prior to installation.

FEC_uncorrectable error insertion

It is also a requirement to test the maximum number of errors a DUT is able to detect. Here, it is not possible for the errors to be corrected by the DUT. The necessity to perform this test feature is identical to that previously mentioned for the FEC_corr feature.

When inserting the FEC_uncorr error, alarms by the DUT can be expected when the DUT is operating correctly.

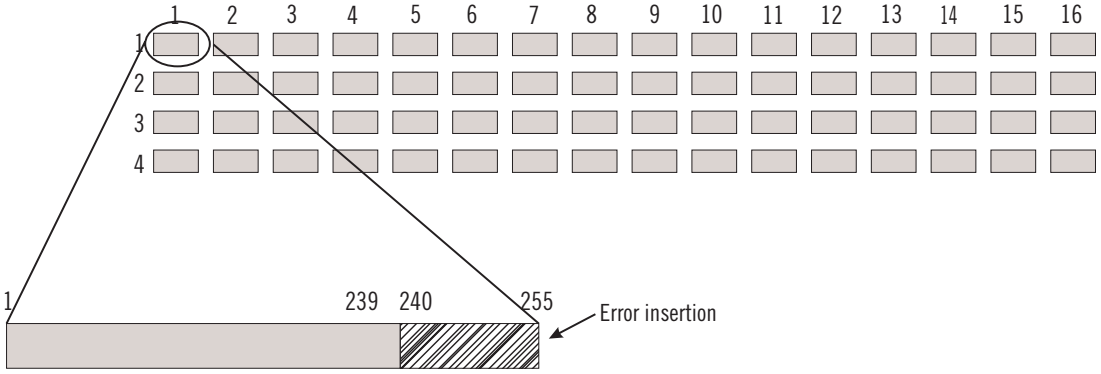

Figure 4: FEC _uncorrectable error insertion

In performing this test, 16 bytes are inverted in the first sub-row of the first OTU-row. This is similar to the byte inversion for the correctable errors, with the exception that all 16 bytes (240 to 255) of the sub-row are inverted.

FEC_maximum error insertion

This functionality allows the user to acquire a PASS / FAIL criteria of the DUTs capability to correct up to 8 symbol errors.

In this case, the ONT-5xx inserts the maximum number of possible byte (symbol) errors which the DUT should still be capable of correcting. In other words, the system is stressed to its maximum. This test inserts errors over the entire OTU frame.

A graphical representation of a sub-row is used to describe in detail error insertion when using FEC (figure 5).

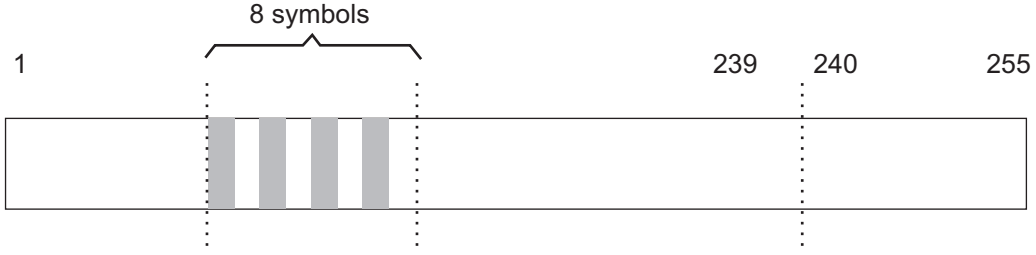

Figure 5: Sub-row illustrating detail error insertion using FEC

Performing the maximum stress test ensures that the following test conditions are met:

- All combinations of byte error masks will be used during error insertion
- A maximum of 8 symbol errors are inserted in each sub-row (figure 5)
- All 16 sub-rows of all 4 OTU-rows will be errored
- All possible byte positions of the whole OTU-frame will contain errors

In order to guarantee that all the bytes of the OTU-frame are errored at least once, the following parameters are determined internally:

- **Starting position of error insertion**
  The starting position of the error insertion is defined from the time the insertion button is pressed

- **Determination of byte error mask**
  Random generation of all possible bit combinations between 0x01 and 0xFF determines which bit in a byte is inverted. This could be for example the following mask: F3 03 A1 B7 7B 04 AB 32, which specifies the position of inversion in the 8 individual errored bytes. This error mask changes continuously resulting in a random sequence of generated symbol errors.
- **Distribution of errored positions**
  Once the starting position of the first 8 symbol errors is determined, the position of the following 8 byte errors are distributed throughout the whole OTU-frame. This guarantees a pseudo-random distribution of errors over the entire OTU frame.

This test setup guarantees that after approximately 3ms of FEC error insertion, every byte in the OTU-frame is errored at least once.

Should the DUT behave correctly under maximum stress test conditions it should be able to correct all errors. The return signal generated toward the ONT-5xx should as a result be free from errors. However, when the ONT-5xx receives errors from the DUT, further testing is necessary using the ONT-5xx's FEC_advanced functionality.

FEC_advanced error insertion

The FEC_advanced functionality implemented in the ONT allows a "microscopic" view of implementation of the FEC algorithm.

FEC_adv is used in:

- R&D when the FEC algorithm is being designed and verified
- Allowing quick pin pointing of failures inside encoder and decoder designs FEC_max is used to test the limit of the DUTs correction capabilities

FEC_advanced is capable of testing below and beyond these limits. To be more specific, it enables the user to define exactly which bit in a particular byte of an OTU-row and sub-row should be errored.

As previously mentioned, the FEC_adv functionality helps define which bit should be errored where in the OTU-frame.

The graph in figure 6 shows the parameters that can be specified in the FEC_adv. feature.

This implemented feature makes it possible to choose the following parameters:

– selection of row

– selection of sub-row

– starting position of burst in the sub-row

– number of errored bytes per sub-row

– specify which bit should be inverted in the selected bytes

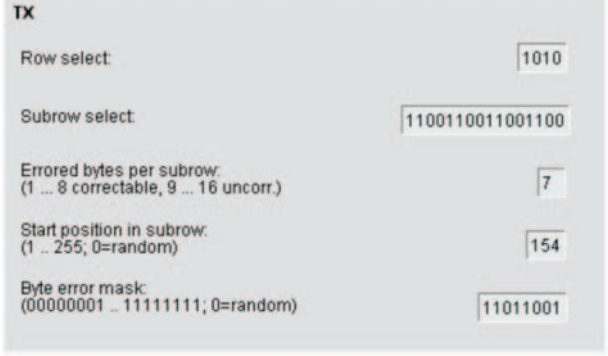

Figure 6: Parameters for specification in FEC_adv feature

A possible scenario for testing the limit and beyond could be:

- Select all 4 OTU rows by choosing for example, 1010
- Select first sub-row, for example, 0000 0000 0000 0001, which means that the first sub-row will be errored in all the OTU-rows
- By selecting the number of errored bytes, the correction capability limit and beyond can be tested. When selecting 8 bytes, the DUT must be able to correct the errors. However, when inserting 9 bytes, the DUT must respond with errors. The selection of the starting position allows the user to specify particular parts of the sub-row to be tested. For example, sections of the FEC part can be errored to put focus on the FEC functionality
- The last parameter specifies the specific bits inverted in the bytes selected within the sub-row parameter. This is a requirement when testing particular sequences of the FEC encoder and decoder on a bit basis.

With careful selection of these parameters, each individual byte can be errored and the resulting behavior be tested.

What to expect when using the various FEC functionalities

Tx error insertion type	**Rx response at ONT-5xx after DUT**
Random error	
FEC_correctable	No errors
FEC_uncorrectable	The ONT-5xx displays count, ratio and seconds of uncorrectable errors in the case of no new FEC being calculated by the DUT
FEC_maximum (stress test)	No errors
FEC_advanced	• No errors when testing the limit of the DUT (see FEC_max testing) • When testing beyond the limit: The received signal at the ONT-5xx is dependent on the configuration of the DUT (e.g. calculation of new FEC, generation of alarms) and the specified insertion position (payload section or FEC section) of the error in the OTU-frame

Summary

The ONT-5xx's FEC functionality provides the user with in-depth FEC testing making the instrument suitbale for use in early development stages, during verification stages, as well as in the installation and maintenance of FEC systems.

The ONT-5xx is the only test solution on the market that delivers this level of FEC testing together with simple, one-button, stress testing funtionality.

Abbreviations

DUT	Device under test
FEC	Forward error correction
FEC_adv	FEC_advanced
FEC_corr	FEC_correctable
FEC_max	FEC_maximum
FEC_uncorr	FEC_uncorrectable
NE	Network element
OTU	Optical channel transport unit

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