One-Way Delay & Jitter Measurement

Key Factors Affecting One-Way Delay Measurement Accuracy

- Test Unit Intrinsic Error
  Resulting from time-stamping accuracy & packet buffering / processing performance
- Clock Synchronization Accuracy
  1-way delay accuracy is greatly affected by the reference clock offset between units

One-Way Delay & Jitter Measurement

One-way delay and delay variation (jitter) measurements are becoming increasingly important as SLAs specify these parameters to ensure the QoS of real-time applications such as VoIP, telepresence and transactional services. Equally stringent in both wireline (Ethernet access) and wireless backhaul networks for 4G (WiMAX / LTE), typical SLA specifications call for unidirectional jitter less than 1-5 ms and latency in the 3-10 ms range.

Service providers are increasingly turning to one-way measurements to assure their SLAs and monitor their services, since round trip delay metrics often fail to identify QoS issues in asymmetrical access networks (download speeds normally exceeding upload). Since a round-trip delay measurement aggregates send and receive path delays, unidirectional issues can escape detection or exacerbate troubleshooting efforts. One-way measurements can quickly identify and quantify these QoS issues, but only if they are conducted with sufficient precision and accuracy.

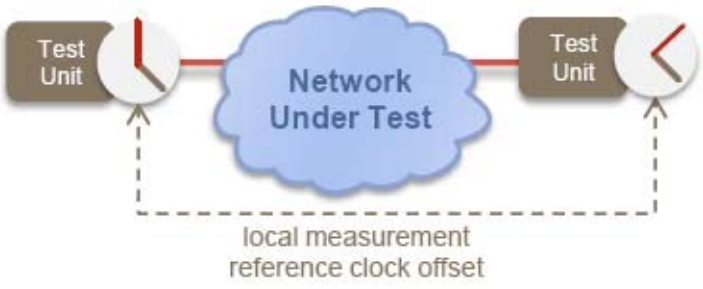
One-Way Delay Measurement

In packet-based networks, one-way delay and jitter are measured by sending a precisely time-stamped test packet across the network under test. To test the delay or jitter of a particular service, the test packet is tagged with the same frame attributes as the packets carrying the service (VLAN, CoS, destination address, etc.) Time-stamping is performed by the originating test unit; the receiving test unit compares the time stamp of the test packet with the time of its reference clock -the difference is the one-way delay. To measure jitter, the variation in one-way delay between subsequent packets is calculated.

Two key factors affect the resolution and accuracy of these one-way measurements: (1) synchronization error between the test units' reference clocks, and (2) the intrinsic error of the measurement device itself. Both of these must be minimized to provide a meaningful one-way delay measurement -if the error approaches even a tenth of a millisecond, the accuracy will be insufficient to reliably detect SLA performance issues.

Reference Clock Sync Errors

Reference clock offset is dependent on the scheme used to synchronize the units. As packet-based networks are asynchronous, there is no standard, network-based timing signal available. As a result, a number of schemes have been developed to distribute a clock sync signal by transmitting reference packets through the network. The most widely used schemes are known as Network Timing Protocol (NTP) or Packet Timing Protocol (PTP), outlined in a number of ITU and IEEE standards.

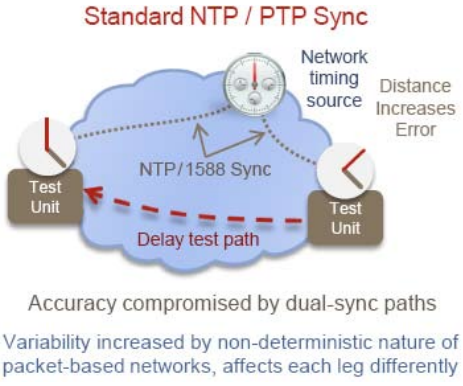


Reference Clock Sync Required for 1-Way Measurements

Although these standards define the protocol by which reference timing signals are transmitted and maintained, the particular implementation used by the measurement units has a significant effect on delay measurement accuracy.

A common approach is to install a NTP / PTP reference timing server (source) in the network, which is then accessed by measurement units to synchronize their reference clocks.

Although widely accepted as a viable sync method, this approach has certain inherent limitations that affect measurement accuracy: (1) the quality of the sync source itself, (2) variability in network congestion, (3) the distance from the timing source to the measurement units.

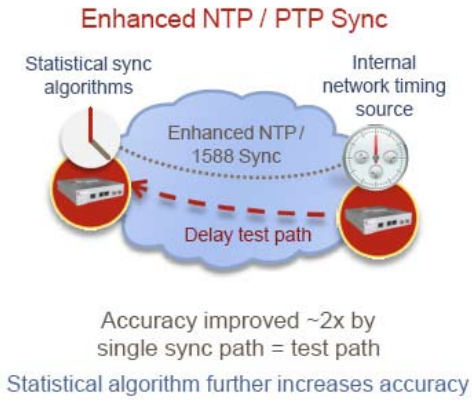


While NTP / PTP algorithms can somewhat mitigate the effects of traffic congestion, timing source location has a significant effects on measurement accuracy since clock sync error increases with both the distance between the measurement units and the timing source, as well as the difference in paths between the service under test and the route taken by the sync packets.

A more reliable and accurate approach addresses these issues by embedding a networking timing source (NTP / PTP) directly into one of the measurement units. This method matches the sync path to the service transport path under test, while also eliminating delays related to accessing a remote time server.

Taking sync accuracy to highest possible level, this technique has been combined with a patent-pending enhanced NTP / PTP statistical sync algorithm that greatly reduces the effects of high frequency delay asymmetries caused by network congestion.

Taken together, this allows EtherNID and MetroNID demarcation units to provide one-way delay and jitter measurements with <20 µs accuracy, and 1 µs resolution -significantly more accurate than other methods, and ideal for assuring SLAs with stringent one-way delay specifications.



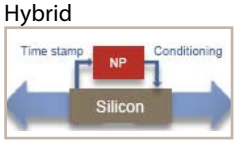
Intrinsic Measurement Error

In addition to clock sync errors, delay measurement accuracy is also affected by the design of the device itself (intrinsic error). Since measurements are based on comparing the time of the receiving unit's reference clock to the time stamp in the test packet received, the processing and time-stamping architecture of the measurement units has a significant and direct effect on measurement accuracy

To obtain the best-possible delay measurement results, time stamping and packet-processing should be performed directly "on the wire". Devices that use store-and-forward buffering algorithms and / or place network processors in the measurement path introduce a variety of errors when stamping and calculating delay and jitter. Such architectures often exhibit intrinsic error in the range of 0.1-1 ms -enough to prevent accurate measurement of high-performance SLA delay metrics.

To minimize intrinsic delay, measurement devices can be designed so that time stamping and packet-processing is done in a dedicated, purpose-built silicon chip. This approach offers such fast processing performance that store-and-forward buffering is not required, and time stamping is essentially performed in real-time, as transparent to traffic as if the device was simply a passive piece of wire This architecture can yield intrinsic errors as low as one microsecond, up to three orders of magnitude more precise than alternative designs.

In-Line Packet Processing & Test Architectures

	Purpose-Built, Pure Si Data Path	Packet Processing	Time-Stamping &Measurement	Pass-Thru Delay	Measurement Resolution*	QoS Impact
JDSU		Real Time "On the Wire"	Hardware "On the Wire"	3.3 µs	<1 µs	NONE
Other NID Manufacturers	Off-the-shelf Network Processor 	Store & Forward Sensitive to Traffic Load	Software-Based Sensitive to Traffic Load	300 µs to 500 µs	100 to 1000 µs	Delay & Jitter introduced to all traffic
	Network Processor Hybrid 	1/2 Only Filtering to NP "On the Wire"	Software-Based/ Store & Forward Measurement and Conditioning Functions	300 µs to 500 µs	100 to 1000 µs	Delay & Jitter introduced to conditioned traffic

* + clock sync error

EtherNID™ & MetroNID™ Demarc Units

JDSUs packet assurance demarcation units' unique Fast-Thru™ architecture and internal NTP / PTP timing source provides advanced 1-way delay and jitter measurements with microsecond resolution -the most accurate available, and ideal for high-performance SLA assurance applications.

Unlike store-and-forward architectures, the Fast-Thru silicon data-path provides wire-speed pass-through performance without adding jitter or delay, while at the same time providing real-time processing of every packet flowing through the unit.

EtherNID™ & MetroNID™ units also feature advanced on-board performance testing and service creation capabilities in a compact, cost efficient, carrier-grade in-line element.

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