VIAVI Solutions

Whitepaper

Dynamic Skew – the key to accelerating product debugging and validation

The VIAVI ONT is a powerful tool with applications in the PHY layer, signal integrity and logic validation. Dynamic Skew is a unique and key application which underpins test and validation for the next generation of Ethernet.

Fractions of a Nanosecond

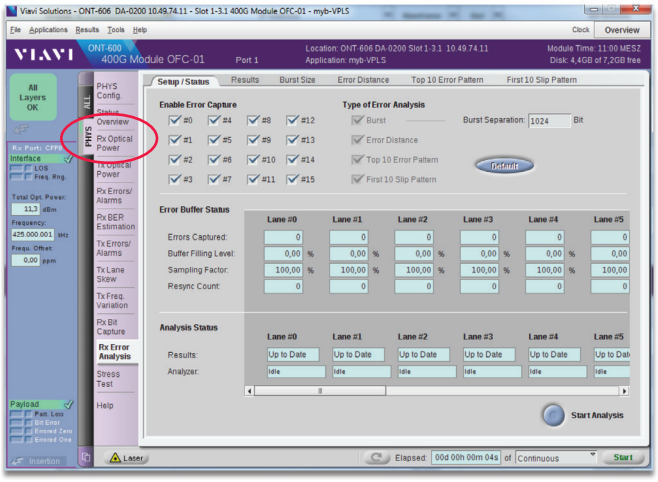
Modern high speed interfaces used in the last generations of Ethernet exist in a world of tiny fractions of a nanosecond, the transition times between individual data bits or symbols is in the realm of picoseconds. Timing sensitivity has become a critical issue for Ethernet at 400Gb/s and beyond. VIAVI has a wealth of experience in this domain. Building on our leadership in 40 Gb jitter, we quickly identified the issues that will challenge future high speed interfaces and used our expertise to build unique and insightful applications. Dynamic Skew is at the heart of validating and troubleshooting the fast parallel interfaces using PAM-4 signaling at 56G and 112G. It quickly highlights issues with CDR margin, clock architecture and fundamental signal integrity like crosstalk.

What is Dynamic Skew?

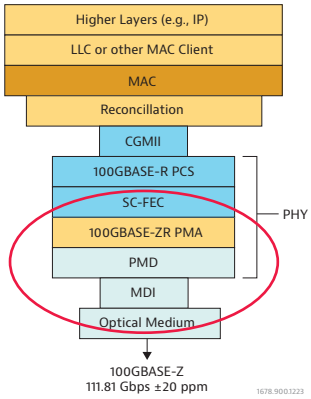
Dynamic Skew is a physical layer phenomenon which occurs in electrical and optical parallel interfaces. Lanes, even on the same clock domain, can have small variations in timing which in the worst case can cause effects such as bit errors, error bursts and link flaps. Tolerance to Dynamic Skew is laid out in IEEE standards for various points within Ethernet interfaces.

The latest generation of 800 Gb Ethernet (802.3 df) uses 8 parallel electrical lanes, each running at 112Gb/s with PAM-4 symbols – each symbol has a duration of under 20 ps so edge placement and transition dominate performance. Since we use parallel fast lanes to carry data between ICs and modules over cables, PCBs and optics, relative time can cause issues. Tiny changes in timing can cause the skew between lanes to vary – especially over time, temperature and operating conditions. To put this in perspective – 1 inch of PCB trace represents 150 picoseconds – nearly 8 complete symbols at 112Gb/s.

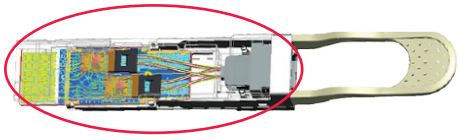
Where is the PHY layer?



PHY layer tab on ONT GUI



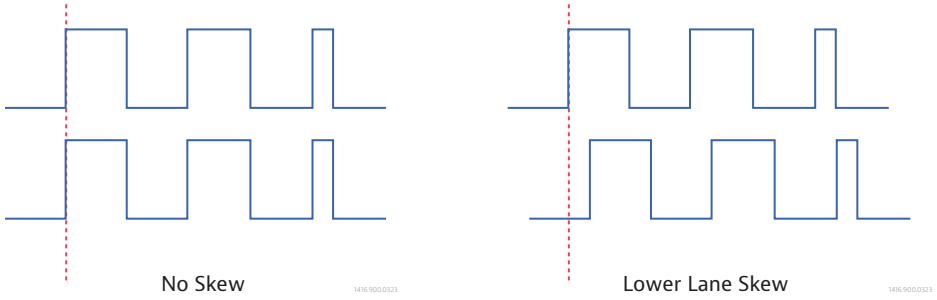
PHY layer in 802.3 stack



X-ray view of QSFP-DD module

What is Skew?

In the image below, we can see a signal being sent over a two-lane parallel interface. In the first case, the lane timing is aligned, and all the transitions (edges) occur together. In the second image, the lower waveform is slightly delayed, so its transition now occurs in the middle of the upper lanes 'bit'.



No Skew

Lower Lane Skew

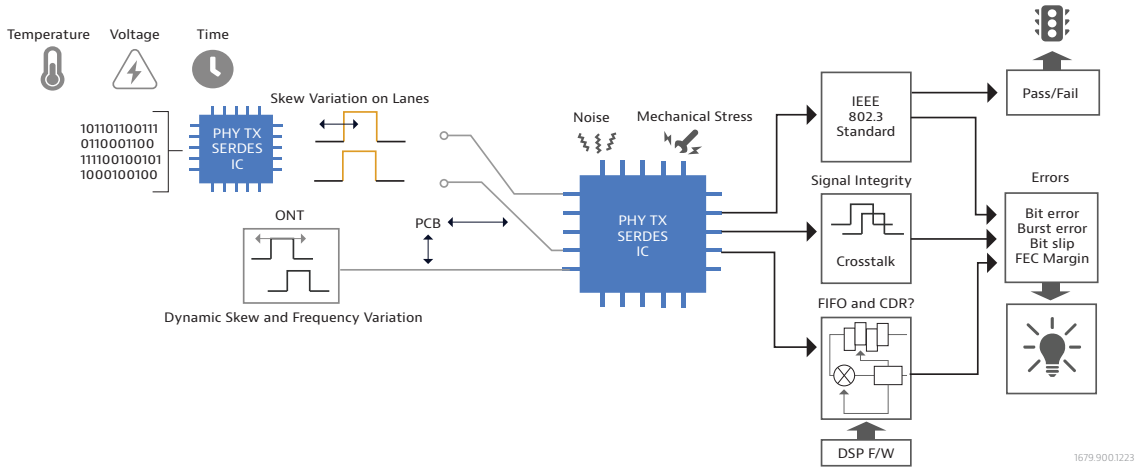
Skew can be caused by thermal, voltage, optical and mechanical effects. We typically measure skew in either picoseconds (psec) or ul (1ul = a complete symbol period).

Dynamic Skew – Cause and Effect

At 53Gb, the timing of signals is critical. For example, 1 symbol is under 40 psec (1 inch of PCB ~ 150 psec). Slight changes in operating conditions, like temperature and voltage, across a parallel link (even in one IC) can cause slight changes in propagation delays in the electrical signal. This 'breathing effect' can cause lanes to dynamically skew back and forth.

Normally, the RX buffers (DLL, FIFO) should absorb this, so the higher lanes are not impacted. If the RX PHY does not absorb the skew, this gives rise to random bit errors and slips which are very difficult to troubleshoot and fix later on. The timing variation can also impact the sensitive clock recovery circuitry based on advanced DSP used extensively in modern PAM-4 SERDES. In worst cases Dynamic Skew causes momentary loss of lock in the CDR leading to elusive troublesome error bursts.

Dynamic Skew has an impact at an even more fundamental level. One of the biggest challenges with modern interfaces and especially board layout is signal integrity. Dynamic Skew is particularly effective at exposing issues around crosstalk – a skew variation may lead to a bit transition from a neighbor lane occurring in the middle of the victim lane eye – degrading the BER for a tiny moment.



Signal integrity challenges and the impact of skew

Static Skew – Cause and Effect

Static Skew occurs in whole symbols (ul) at PCS layer (logic). It should not change after a link is up and running. Static Skew causes include:

- Delays in FIFOs
- Gearbox path delays and lane assignments

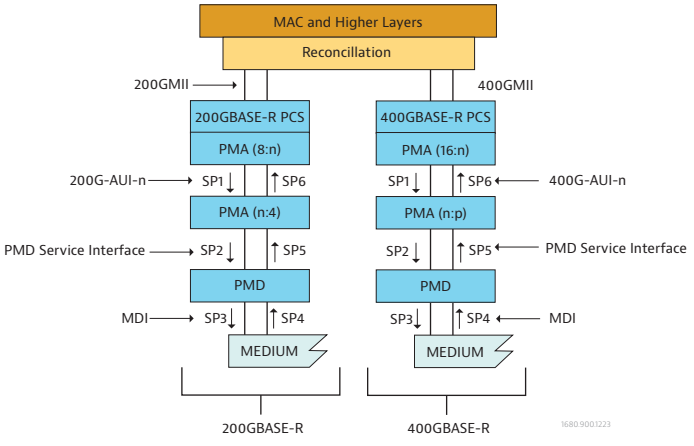
The PCS layer corrects this skew by reading the VL lane alignment marker and working out where that lane should be. Buffer memory in the PCS receiver is used to realign the VL lanes and create the Ethernet frame. Issues occur if the relative skew (earliest to latest VL) exceeds the capacity of the buffer memory. Corrupted VL lane markers can also cause issues.

The VIAVI ONT can accurately and stably generate Dynamic and Static Skew to aid debugging and validation of high-speed optical modules and interfaces. This, combined with other unique applications gives the VIAVI ONT the ability to quickly identify issues which impact performance, often accelerating validation times from days to a few seconds.

IEEE Skew Constraints

Skew Points	Maximum Skew (ns)[a]	Maximum Skew for 200GBASE-R or 400GBASE-R PCS Lane (UI)[b]
SP1	29	≈770
SP2	43	≈1142
SP3	54	≈1434
SP4	134	≈3559
SP5	145	≈3852
SP6	160	≈4250
At PCS receive	180	≈4781

Summary of Skew Constraints



IEEE diagram showing various skew measurement reference points

Excerpt From IEEE 802.3 re: Bit-Level Multiplexing

...the PMA provides bit-level multiplexing in both the Tx and Rx directions...The aggregate signal carried by the group of input lanes or the group of output lanes is arranged as a set of PCSLs/FECLs..... Each PCSL/FECL is mapped from a position in the sequence on one of the **m** input lanes to a position in the sequence on one of the ***n*** output lanes. If bit ***x*** sent on an output lane belongs to a particular PCSL/FECL, the next bit of that same PCSL/FECL is sent on the same output lane at bit position ***x + (z/n)***. The **PMA shall maintain the chosen sequence of PCSLs/FECLs on all output lanes** while it is receiving a valid stream of bits on all input lanes.

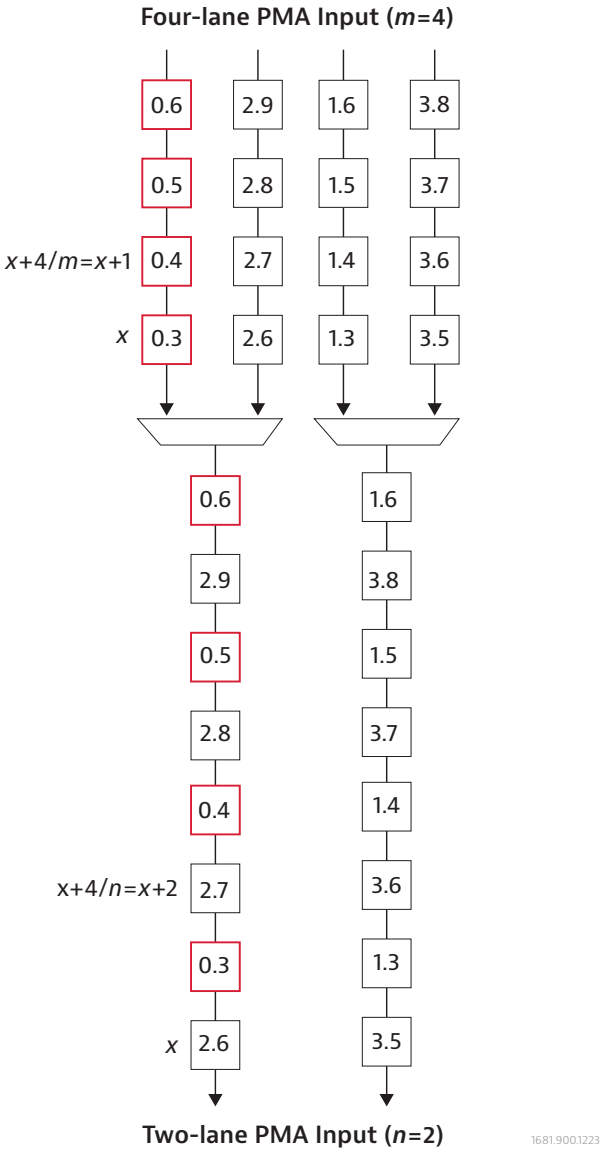


Illustration of lane bit muxing

Dynamic Skew Variation

TX PCSL/FECL Skew Variation

- No external clock required
- Configurable as 26.5625 GBd lane pairs <0,1><2,3><4,5><6,7>
- 200GAUI-4 and 400GAUI-8 test application use case support

User defined parameters

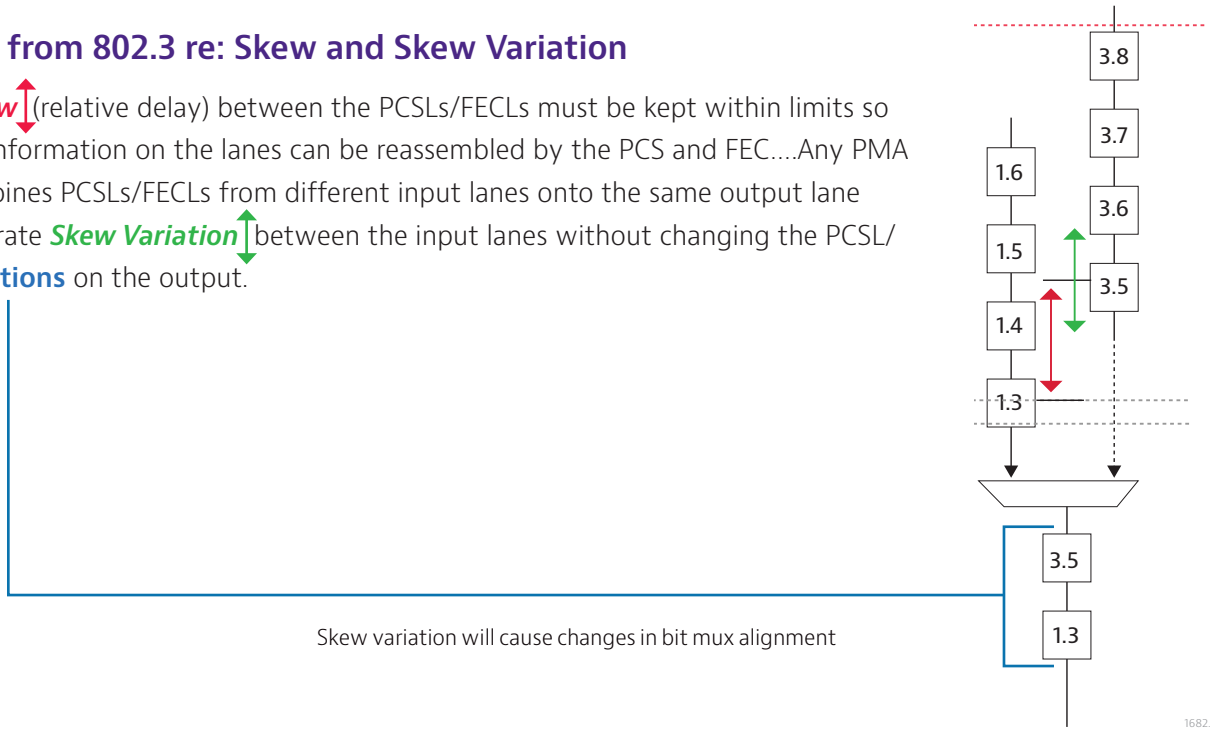
- Amplitude (±512 UI)
- Slope/skew rate
- Step size (res. 10 mUI)
- Peak value
- Manual and triangle mode

IEEE 802.3

- Clause 116.5 and clause 120.5.3
- Skew variation defined as the change in skew between any PCSL and any other PCSL over the entire time that the link is in operation
- May be introduced due to variations in electrical, thermal, or environmental characteristics
- Table 116–8 'Summary of Skew Variation constraints

Excerpt from 802.3 re: Skew and Skew Variation

...The ***Skew*** (relative delay) between the PCSLs/FECLs must be kept within limits so that the information on the lanes can be reassembled by the PCS and FEC....Any PMA that combines PCSLs/FECLs from different input lanes onto the same output lane must tolerate ***Skew Variation*** between the input lanes without changing the PCSL/FECL **positions** on the output.



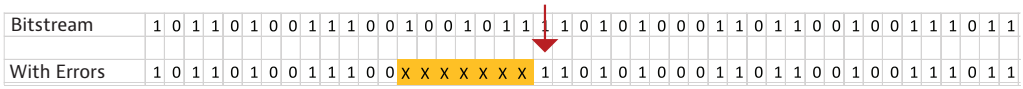
Skew variation will cause changes in bit mux alignment

1682.900.1223

Errors in the Bitstream – Error Burst vs. Bit Slip

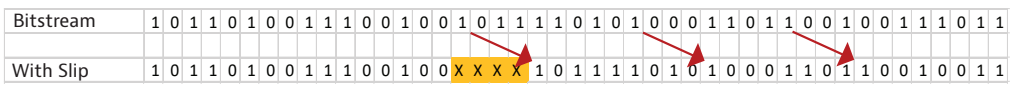
One of the main errors that Dynamic Skew can cause is an error burst – but in reality – an error burst may be two different things, each with a very different root cause. A true error burst is where a sequence of symbols or bits have been corrupted – crosstalk and other signal integrity issues are often the cause. A bit slip is far more elusive. Most T&M cannot distinguish between a burst and bit slip, just recoding it as a burst of errors. The VIAVI ONT has the ability to detect the timing offset, the fingerprint of a bitslip – an indication of issues in timing, especially around the CDR and clocking. Without the ability to tell the difference between error bursts and slips, it is almost impossible to know where to start troubleshooting.

Bursts
- Dynamic Skew
- Crosstalk
- External noise
- Signal Integrity



Sequence has a burst of errors but after error burst the bit sequence remains aligned.

Bit Slips
- Dynamic Skew
- Incorrectly 'tuned' CDRs
- SERDES
- Equalizer



Sequence has a burst of errors but after error burst is over the bit sequence has an 'offset' – it is a bit slip. The burst is occurring during the slip as a FIFO realigns.

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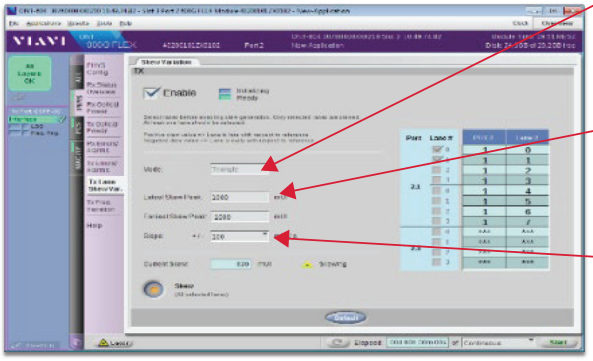
Bit slips and bursts have different causes and impacts on the data lanes

Running a Dynamic Skew Test

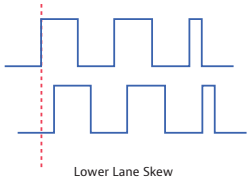


Mode: this selects how the skew is applied – the normal case is a triangle or sawtooth wave that sweeps between the set bounds at the rate selected.

The skew peak sets the earliest and latest skew offset with respect to the unskewed static lanes. These values would normally be set to the limits proscribed by standards.

The rate of the skew variation is not set in standards so the user can try a range of values to see if any difference in behaviour is seen. It may be some DUTs fail at slower skew rates!

ONT GUI for skew variation



Skew variation illustration

The ONT family can support a range of Dynamic Skew insertion rates and capabilities – from 10G NRZ through to the very latest 56 Gbd PAM-4

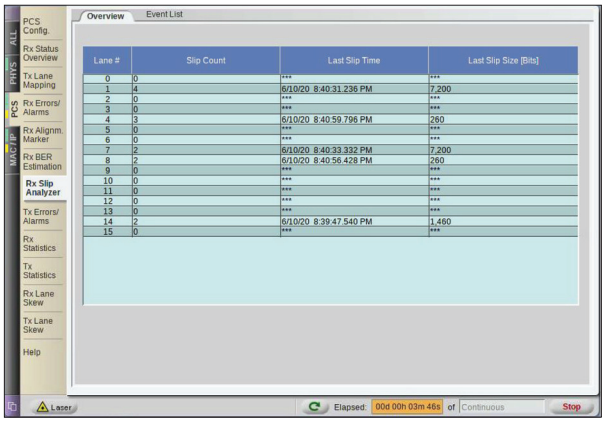
Results and Where to Start troubleshooting

- Bit slips
  - Clock and CDR, Equalizer
  - Timing issues
  - Clock architecture
- Error burst
  - Crosstalk
  - Signal integrity
  - Logic issues

400Gb Bit Slip Analyzer

Conventional BER test sets may be able to identify error bursts but cannot distinguish this from a bit slip. Bit slips have a different cause than classic error bursts, and the ability to distinguish them is critical.

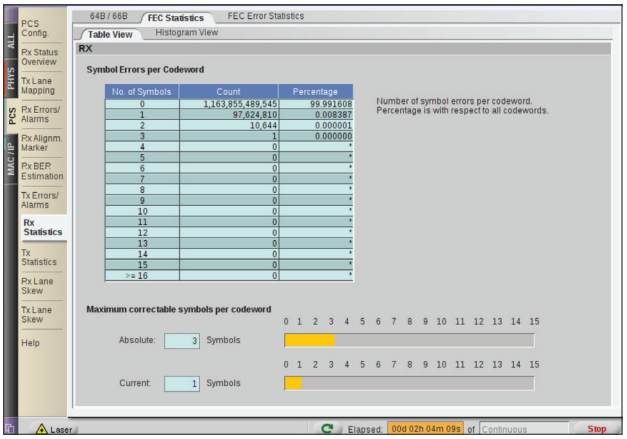
Bit slips are usually due to a CDR losing lock and slipping and then recovering. This per lane view can be done together with Dynamic Skew to indicate susceptibility to skew variation.



ONT GUI showing bit slip analysis

Good FEC Tail – Not Impacted by Dynamic Skew

Without Dynamic Skew this module behaves as expected. The FEC tail is short and monotonic. It drops rapidly with each higher errored symbol count several orders of magnitude less than the previous symbol count.

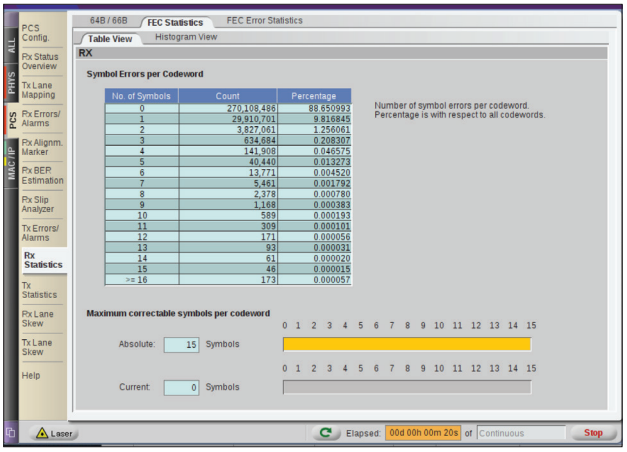


ONT GUI with 'good' FEC tail

Impact of Dynamic Skew – Excessive FEC Tail

When the module is subjected to Dynamic Skew, the DSP CDR inside the module cannot track the excessive skew. This gives rise to a very long FEC tail which hints at long bursts.

The user can the adjust the range and rate of skew to investigate the impact.



ONT GUI with bad FEC tail - long tail

Conclusion

Modern high speed interfaces live in realm of sub nanoseconds. Dynamic Skew is a powerful application that not only ensures interfaces comply to the relevant IEEE 802.3 standards, but also accelerates troubleshooting in the phy layers and ensures complex functional blocks like CDR work under all operating conditions.

The VIAVI ONT offers a unique integrated blend of Dynamic Skew generation coupled with insightful error analysis and fingerprinting applications which work with both unframed and framed traffic.

Elusive timing events that may take hundreds of temperature and restart cycles can be generated in a controlled and consistent manner. This allows insightful analysis to understand the root cause and quickly and confidently resolve the issues to deliver stable, robust products with significant operating margin.

Discover ONT 800G FLEX XPM today!

Are you ready to take the next step with one of our Optical Transport products or solutions? Complete one of the following forms to get going:

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- Request a demo

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