SKB SERIES
FIBEROPTIC SWITCH MODULE

User Manual

JDS Uniphase

ii

Getting Help

For more information, contact JDS Uniphase or your local sales representative.

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Refer to the JDSU Terms and Conditions of Sale for warranty coverage information.

iv

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13.2 JDSU shall not be liable for any delay or failure in performance whatsoever due to acts of God, earthquakes, shortage of supplies, transportation difficulties, labor disputes, riots, war, fire, explosion, epidemics, or other occurrences beyond JDSU's reasonable control or due to unforeseen circumstances.

13.3 Waiver by JDSU of any provision herein must be in writing and shall not be deemed to be a waiver of such provision in the future or of any other provision.

13.4 Customer shall hold confidential and shall not use, disclose or permit others to use any confidential information identified as such in writing or orally by JDSU or information which Customer knows or ought to reasonably know is confidential, proprietary or trade secret information of JDSU, including, without limitation, trade secrets embodied in Products.

13.5 Neither this Agreement nor any rights under this Agreement, other than monies due or to become due, shall be assigned or otherwise transferred by Customer (by operation of law or otherwise) without the prior written consent of JDSU. This Agreement shall bind and inure to the benefit of the successors and permitted assigns of the parties.

13.6 In the event that any of the terms of this Agreement, apart from payment, become or are declared to be illegal by any court of competent jurisdiction, such terms shall be null and void and shall be deemed deleted from this Agreement, but only to the extent that such term is illegal, it being the intent and agreement of the parties that the Agreement shall be deemed amended by modifying such term to the extent necessary to make it legal while preserving its intent or, if that is not possible, by substituting therefor another term that is legal and achieves the same objective. All remaining terms of this Agreement shall remain in full force and effect.

13.7 Neither party has the right or authority to, and shall not, assume or create any obligation of any nature whatsoever on behalf of the other party or bind the other party in any respect whatsoever.

13.8 JDSU neither assumes nor authorizes any third party, person or entity to assume or accept any liability or obligation, or to make any commitment for JDSU with regard to JDSU services or the Products.

13.9 This Agreement constitutes the entire agreement between the parties hereto concerning the subject matter of this Agreement, apart from existing non-disclosure agreements, and there are no understandings, agreements, representations, conditions, warranties, or other terms, express or implied, which are not specified herein. This Agreement may only be modified by a written document executed by authorized representatives of JDSU and Customer.

Contents

7   Contents

List of Figures

9   List of Figures

List of Tables

11   List of Tables

Safety Information, Instructions, and Symbols

Safety Information

Power Requirements

The unit can operate from a DC power source that supplies 5 V. The maximum power consumption is 1 to 2.5 A, depending on the configuration.

Safety Instructions

The following safety instructions must be observed whenever the unit is operated, serviced, or repaired. Failure to comply with any of these instructions or with any precaution or warning contained in the user's manual is in direct violation of the standards of design, manufacture, and intended use of the unit. JDS Uniphase assumes no liability for the customer's failure to comply with any of these safety requirements.

Before Initializing and Operating the Unit

- Inspect the unit for any signs of damage, and read the user's manual thoroughly.
- Install the unit as specified in the Getting Started section on page 11.
- Ensure that the unit and any devices or cords connected to it are properly grounded.

Operating the Unit

⚠	**Warning** To avoid the risk of injury or death, always observe the following precautions before initializing the unit: • If using a voltage-reducing autotransformer to power the unit, ensure that the common terminal connects to the earthed pole of the power source. • Do not interrupt the protective earth grounding. Any such action can lead to a potential shock hazard that can result in serious personal injury. If an interruption to the protective grounding is suspected, ensure that the unit remains inoperative. • Never look into the end of an optical cable connected to an optical output device that is operating. Laser radiation is invisible, and direct exposure can severely injure the human eye. For more information, see the user's manual of the laser source in use. • Turning off the power to the device does not always block the externally supplied radiation to the connector at the output of the unit. • Do not use the unit outdoors. • To prevent potential fire or shock hazard, do not expose the unit to any source of excessive moisture. • Do not operate the unit when its covers or panels have been removed. • Unless absolutely necessary, do not attempt to adjust or perform any maintenance or repair procedure when the unit is opened and connected to a power source. • Repairs are to be carried out only by a qualified professional. • Do not attempt any adjustment, maintenance, or repair procedure to the unit's internal mechanism if immediate first aid is not accessible. • Disconnect the power from the unit before adding or removing any components. • Operating the unit in the presence of flammable gases or fumes is extremely hazardous. • Do not perform any operating or maintenance procedure that is not described in the user's manual. • Some of the unit's capacitors can be charged even when the unit is not connected to the power source.

Safety Symbols

The following symbols and messages can be marked on the unit (Table 1). Observe all safety instructions that are associated with a symbol.

Table 1: Safety Symbols

Symbol	Description
⚠ (laser)	Laser safety. See the user's manual for instructions on handling and operating the unit safely.
⚠	See the user's manual for instructions on handling and operating the unit safely.
⚠ (ESD)	Electrostatic discharge (ESD). See the user's manual for instructions on handling and operating the unit safely.
⏚	Frame or chassis terminal for electrical grounding within the unit.
⏚ (protective earth)	Protective conductor terminal for electrical grounding to the earth.
WARNING	The procedure can result in serious injury or loss of life if not carried out in proper compliance with all safety instructions. Ensure that all conditions necessary for safe handling and operation are met before proceeding.
CAUTION	The procedure can result in serious damage to or destruction of the unit if not carried out in compliance with all instructions for proper use. Ensure that all conditions necessary for safe handling and operation are met before proceeding.

Introduction

General Information

This user's manual for the SKB Series Fiberoptic Switch Module contains complete operating instructions.

The SKB modular 1xN controllable switch controls up to four 1xN optical switches, with configurations up to 100 channels. Small and rugged, the switch is designed to be used in embedded applications. It is available in single-mode (SM) and multimode (MM) versions. It has several features that reduce installation and support efforts. The switch offers low insertion loss and is independent of data format and direction (bidirectional).

Figure 1: SKB Switch

The standard single-pole configuration consists of a single-common port that can be aligned to any one of 26 ports. In electrical terms, the SKB switch is a single-pole, 26-throw switch. The switching mechanism uses collimating lenses that eliminate problems associated with modal noise, and provide low insertion loss and high repeatability.

The SKB Series Fiberoptic switch is backward compatible with the JDS Uniphase SK Series Fiberoptic Switch Module and SP Series Fiberoptic Switch Module.

The switch provides the capability of readable switch parameters.

The optics can be internally connected to provide custom solutions at the customer's request.

Configurations

The SKB switch is configurable. Examples, shown in Figure 2, include

- A single switch with 1xN configuration for N up to 100
- Up to four 1xN switches with a total channel count of up to 100 (for example, four 1x25 switches, two 1x50 switches, and so on)
- Up to two MxN blocking switches for a total M+N channel count of 100 (for example, two 25x25 switches, one 50x50 switch, and so on)
- 1xN switches plus relay switches and passive devices, such as couplers (for example, two 1x25 stepper motor switches with two relay switches and couplers)
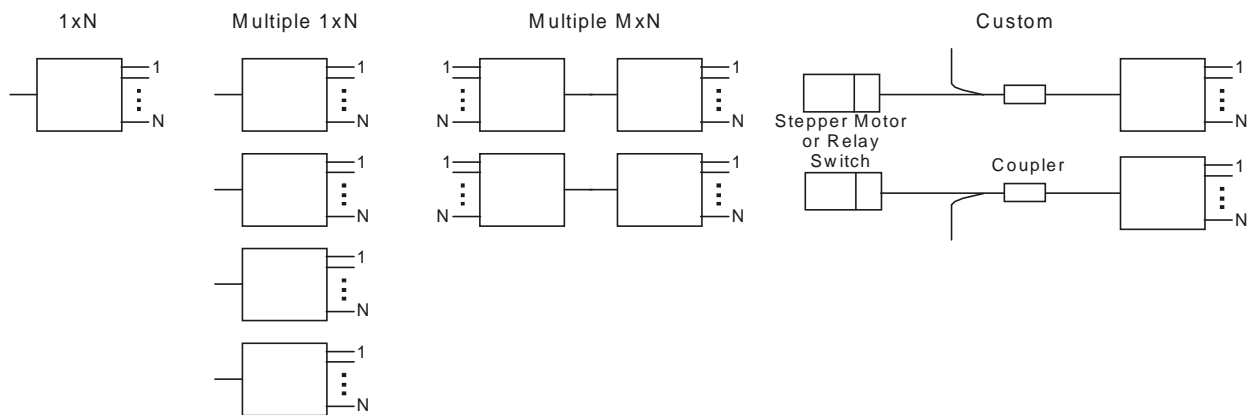
Figure 2: Configuration Examples

A 1xN configuration is shown more closely in Figure 3.
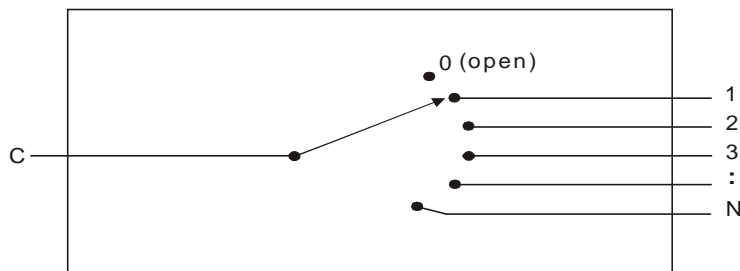
Figure 3: 1xN Configuration

Key Features

- Up to 100 channels
- Typical insertions loss 0.4 dB (multimode) for up to 26 channels
- Parallel and RS485 serial interface control
- Compact modular package suitable for original equipment manufacturing (OEM)

Packages

The SKB switch is available in two package configurations:

- Package 1 can accommodate up to two 1xN switches with a single control interface
- Package 2 can accommodate up to four 1xN switches with a single control interface

Components

For large channel count switches, a high-precision stepper motor is used to align optical channels. The use of collimating lenses minimizes insertion loss.

For some applications, optional relay-based switches can be used.

Passive devices can be incorporated on a custom basis.

Applications

- Remote fiber test systems in telecommunications networks
- Fiber network restoration
- Fiberoptic component test and measurement
- Integration into new products

Standard Accessories

- 3 mm fiber cables or 900 μm fiber pigtails (customer specified)
- User's manual

Latching and Non-Latching

Latching and non-latching SKB switches have the same functionality, command set, and specifications, with the following differences:

- At power off, the non-latching version does not guarantee an optical connect
- When reapplying power to the SKB switch, a latching version stays on the latched channel and a non-latching version resets to a configured known position

Specifications

Table 2 describes the warranted characteristics of the unit. Supplementary specifications describe the typical non-warranted performance of the unit (Table 3).

Table 2: Optical Specifications[1,2,3]

Parameter	Typical (Maximum) N<26 Non-Latching N<25 Latching	Typical (Maximum) 26≤N≤100 Non-Latching 25≤N≤92 Latching

Insertion loss
  SM
  MM
	0.5 (0.7) dB
	0.4 (0.6) dB
		0.8 (1.2) dB
		0.7 (1.0) dB

Wavelength
  SM
  MM
	1290 to 1670 nm
	850 to 950 nm or 950 to 1350 nm
		Wavelength
		  SM
		  MM

Return loss
  SM
  MM
	62 (57) dB
	25 (20) dB
		55 (45) dB
		20 (20) dB

Polarization dependent loss (SM)	0.02 (0.04) dB	0.04 (0.08) dB
Insertion loss stability[4]	±0.02 (0.025) dB	±0.03 (0.04) dB

Table 2: Optical Specifications[1,2,3] (Continued)

Change in insertion loss during power on-off cycle; latching version 　　SM 　　MM	 ±1.0 (2.0) dB ±1.0 (2.0) dB	 ±2.0 (4.0) dB ±2.0 (4.0) dB
Repeatability[5] 　　sequential switching 　　random switching	 ±0.005 (0.01) dB ±0.01 (0.05) dB	 ±0.01 (0.03) dB ±0.03 (0.08) dB
Crosstalk	-90 dB	-80 dB
Switching time (one channel/each additional channel) 　　low speed, high accuracy 　　medium speed	 25/15 ms 20/15 ms	
Optical input power	300 mW continuous	Optical input power
Lifetime	At least 10 million cycles	Lifetime
Interface	Parallel and RS485 serial	Interface

1.	All specifications referenced without connectors.
2.	All optical measurements taken after temperature has stabilized for one hour.
3.	All specifications are at low speed setting. Repeatability can be affected by increasing speed.
4.	Return loss specifications based on 1 m pigtail length.
5.	Repeatability measured after one-hour warm-up.

Table 3: Other Specifications

Electrical	
Input voltage	5 ±0.25 V DC
Power consumption	1 to 2.5 A maximum, configuration dependent
Physical	
Dimensions (W x H x D) 　　package 1 fiber version 　　package 1 cable version 　　package 2 fiber version 　　package 2 cable version	 7.82 x 2.78 x 14.00 cm (3.08 x 1.095 x 5.51 in) 7.82 x 2.78 x 17.17 cm (3.08 x 1.095 x 6.76 in) 13.84 x 2.78 x 14.00 cm (5.45 x 1.095 x 5.51 in) 13.84 x 2.78 x 17.17 cm (5.45 x 1.095 x 6.76 in)
Weight	depends on configuration 0.6 kg maximum for package 1 configuration 1 kg maximum for package 2 configuration
Environmental	
Operating temperature	-35 to 75 °C
Storage temperature	-40 to 85 °C
Humidity	maximum 95% RH, non-condensing, from -35 to 75 °C

Channel Switching Times

The time to a sequential channel (for example, going from channel two to three) can appear to be greater than the specification for the adjacent channel. This discrepancy can be due to a few reasons:

- If the user has used the REPLACE command to replace a damaged channel, that channel is not sequential. Management of the switching order can be done using the SWAP_CHANNEL command.
- The factory configuration can be such that a channel was deliberately skipped.

Confirming Time Between Channels

The SKB switch allows the user to confirm the specified time to switch between channels. The CONNECTION_TIME? query physically checks the time by switching between the start and destination channel. The query output is the time as calculated using the internal clock.

Getting Started

The SKB Series Fiberoptic Switch Module package consists of the switching unit with fiber pigtails and a user's manual. An evaluation kit with software and cables is available for testing the operation of the switch.

Before Initializing and Operating the Unit

- Inspect the unit for any signs of damage.
- Read the user's manual thoroughly, and become familiar with all safety symbols and instructions to ensure that the unit is operated and maintained safely.

Initial Inspection
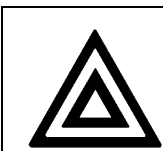
	Warning
	- To avoid electrical shock, do not initialize or operate the unit if it bears any sign of damage to any portion of its exterior surface, such as the outer cover or panels.

Check that the unit and contents are complete:

1. Wear an anti-static wrist strap and work in an electrostatic discharge (ESD) controlled area.

2. Inspect the shipping container for any indication of excessive shock to the contents, and inspect the contents to ensure that the shipment is complete.

3. Inspect the unit for structural damage that can have occurred during shipping.

4. Keep the packaging.

Immediately inform JDS Uniphase and, if necessary, the carrier if the contents of the shipment are incomplete, if the unit or any of its components are damaged or defective, or if the unit does not pass the initial inspection.

Operating Environment

In order for the unit to meet the warranted specifications, the operating environment must meet the following conditions for temperature and humidity.

Temperature

The unit can be operated in the temperature range of -35 to 75 °C.

Humidity

The unit can be operated in environments with up to 95% humidity, non-condensing (-35 to 75 °C). Do not expose it to any environmental conditions or changes to environmental conditions that can cause condensation to form inside the unit.

	Warning
⚠	• Do not use the unit outdoors.
	• To prevent potential fire or shock hazard, do not expose the unit to any source of excessive moisture.

Storing and Shipping

To maintain optimum operating reliability, do not store the unit in locations where the temperature falls below -40 °C or rises above 85 °C. Avoid any environmental condition that can result in internal condensation. Ensure that these temperature and humidity requirements can also be met whenever the unit is shipped.

Claims and Repackaging

Immediately inform JDS Uniphase and, if necessary, the carrier, if

• The contents of the shipment are incomplete
• The unit or any of its components are damaged or defective
• The unit does not pass the initial inspection

In the event of carrier responsibility, JDS Uniphase will allow for the repair or replacement of the unit while a claim against the carrier is being processed.

Returning Shipments to JDS Uniphase

JDS Uniphase only accepts returns for which an approved Return Material Authorization (RMA) has been issued by JDS Uniphase sales personnel. This number must be obtained prior to shipping any material to JDS Uniphase. The owner's name and address, the model number and full serial number of the unit, the RMA number, and an itemized statement of claimed defects must be included with the return material.

Ship return material in the original shipping container and packing material. If these are not available, typical packaging guidelines are as follows:

1. Wear an anti-static wrist strap and work in an ESD controlled area.

2. Wrap the unit in anti-static packaging. Use anti-static connector covers, as applicable.

3. Pack the unit in a reliable shipping container.

4. Use enough shock-absorbing material (10 to 15 cm or 4 to 6 in on all sides) to cushion the unit and prevent it from moving inside the container. Pink poly anti-static foam is recommended.

5. Seal the shipping container securely.

6. Clearly mark FRAGILE on its surface.

7. Always provide the model and serial number of the unit and, if necessary, the RMA number on any accompanying documentation.

8. Please contact the RMA department, using the contact information at the beginning of this document, to provide an RMA number and a shipping address.

Cleaning Connectors

⚠	**Caution** • Connecting damaged or dirty fibers to the unit can damage the connectors on the unit. • Never force an optical connector. Some connectors have a ceramic ferrule that can easily be broken.

Optical cable ends need to be cleaned before using them with the unit.

The following items are required for cleaning:

*   Filtered compressed air or dusting gas
*   Lint-free pipe cleaners or lint-free swab
*   Lint-free towels
*   Optical grade isopropyl alcohol or optical grade 200° ethanol (do not use rubbing alcohol, which contains 30% water)

To clean the connectors:

1. Blow the sleeve with filtered compressed air (Figure 1)
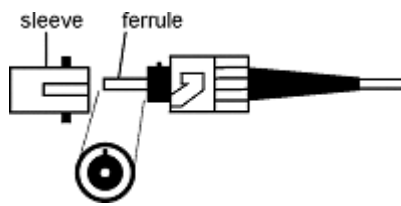
Figure 1: Connector Cleaning (connector type can vary)

2. Apply optical grade isopropyl alcohol or optical grade ethanol to a small area of a lint-free towel and rub the end of the ferrule over the wet area.

3. Wipe the ferrule on a dry area of the lint-free towel.

4. Using the dusting gas or compressed air, blow the end of the ferrule.

5. Apply the alcohol or ethanol to a lint-free pipe cleaner or swab and wipe off the remaining parts of the connector.

6. With the other end of the pipe cleaner or swab, dry the areas cleaned.

7. Using the dusting gas or compressed air, blow the areas cleaned.

Storing Fiberoptic Connectors

All fiberoptic connectors are shipped with dust caps installed on the connectors. Keep the dust caps on the connectors whenever the fiberoptic connectors are not mated.

Handling Fiberoptic Cables

The SKB switch can be shipped with fiber pigtail outputs. These pigtails must be handled with care to avoid damage.

⚠️	**Caution** • Do not bend the pigtails with a radius under 4 cm (1.5 in). A small bend radius adversely affects the optical performance of the pigtail and leads to early failure of the pigtail.

Installation and Physical Interface

Overview of Physical Interfaces

In order to support the various implementations demanded by the OEM market, the SKB Series Fiberoptic Switch Module offers various control and power interfaces/ protocols. All interfaces/ protocols documented in this manual are present on the SKB connector.

Example of typical applications and methods of implementation are provided (for the power and communication interfaces) in the section on Operation and Control.

Physical Interface

Physical Interface: The SKB Connector

A 50 pin male connector services both parallel and serial communication interfaces (JDS part number S010604).

The connector on the SKB switch is an IDE, 50(2x25) male + 4 male power, PCB, edge-mount connector, (Comm Con P/N 7514).The recommended mate for SKB operation is an IDE, 50(2x25) female + 4 female power, right angle connector (Comm Con P/N 7510).The recommended mate for SK emulation is a 2x13 female ribbon connector.

For details on pin numbering and connector dimensions, please refer to Figure 2 and Figure 3 respectively. For further information about connector specifications, please contact:

Comm Con Connectors, Inc.
1848 Evergreen Street, Duarte, CA 91010
Phone: (626) 301-4200 Fax: (626) 301-4212
Email: info@commcon.com
Home Page: http://www.commcon.com
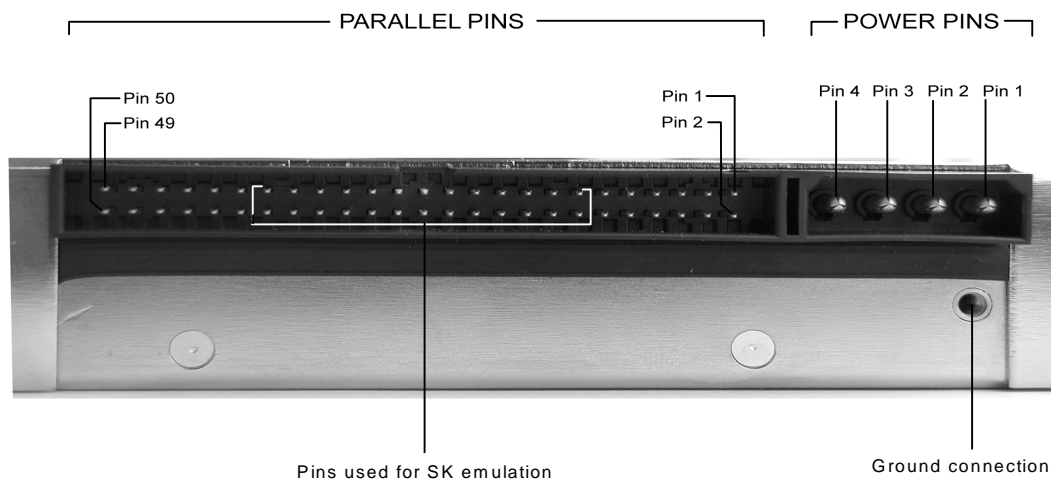
Figure 2: The IDE 2x25 Connector on an SKB Switch
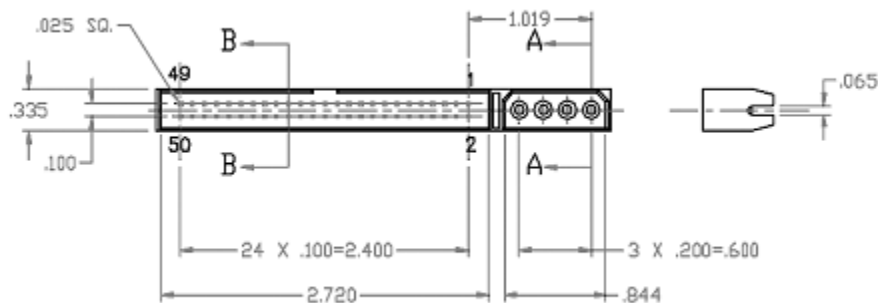
Figure 3: SKB Switch IDE Connector Dimensions

Physical Interface: Connecting to the SKB Connector

The typical application makes use of a 50 strand flat ribbon cable with a crimped 50-pin (25x2) IDE HDD connector. However, in Simplex (SK/SP emulation), a 26 pin flat cable and crimped connector (13x2) would be used in order to make it backwards compatible with existing products.

Depending on customer applications and requirements the following connectors are recommended:

1. Connect to the SKB with PCB-PCB interface:

    From Comm Con Connectors Inc. (http://www.commcon.com/main/drive-mate-connectors.html)
    *   50 + 4 position straddle mount (p/n 7513)
    *   50 + 4 position straight (p/n 7512)
    *   50 + 4 position right angle - Reversed (p/n 7511)
    *   50 + 4 position right angle (p/n 7510)

2. Connect to the SKB by ribbon connectors:

From Thomas & Betts Corporation (http://www.thomasandbetts.com)
- 2x25 connector: 622-5041, 636-5041

Power connectors from Molex Inc. (http://www.molex.com/cgi-bin/bv/molex/index_login.jsp)
- Connector housing 1x4: 15-24-4048
- Crimp terminal: 02-08-1204

3. In Simplex (SK/SP Emulation), a 26 pin ribbon cable connectors:

From Thomas & Betts Corporation (http://www.thomasandbetts.com)
- 622-2641, 636-2641

A right angled PCB mounted connector (25x2) may also be used in order to eliminate any harnessing/ cabling. (JDS Uniphase part numbers 10115117 and 10115118)

Physical Mounting and Connection

To install the switch:

1. Mount the chassis using the four holes provided. An M3 screw with maximum thread depth in the unit of 5 mm is recommended.

2. Connect the ground lug to chassis ground. An 8 mm depth M3 screw with flat and lock washers is recommended (5 mm maximum thread depth in unit). See Figure 4, showing location of mounting holes for both package sizes (note the additional length of package for cable version of switches).

3. Connect the power supply to the unit via the selected interface (See the Pinout Information for the Switch section on page 18 for more information.). A supply of 5 V ±5%, 1 to 2.5 A maximum (configuration dependent), is required.

4. Connect a flat ribbon cable or rigid PCB connector to the unit (see the following sections for the appropriate pinout). The switch is now ready for use.

For information on installing multiple SKB switches in a network, see the Connecting Multiple Switches using the RS485 Interface section on page 26.
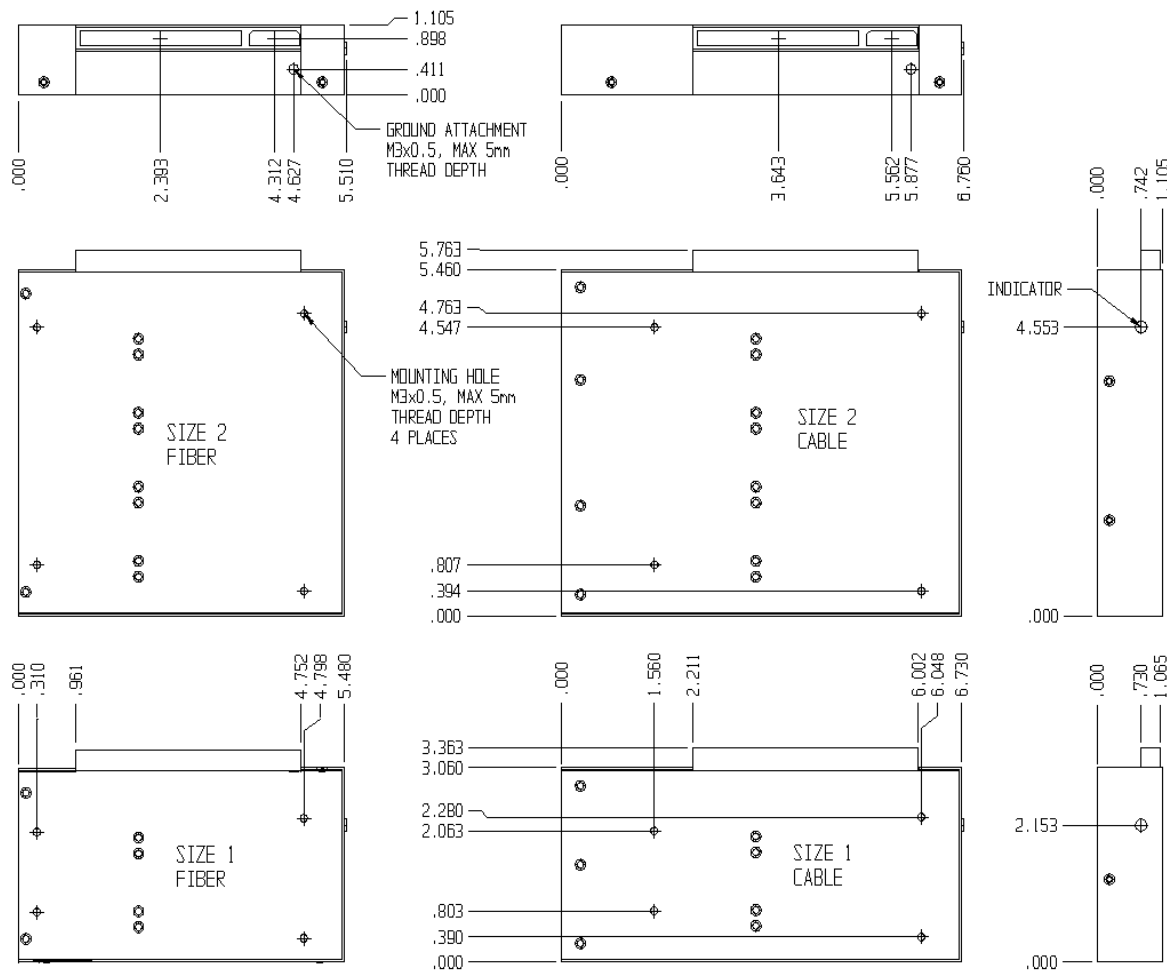
Figure 4: Additional Dimensions

Operating and Maintenance Instructions

Pinout Information for the Switch

The signals for communication are connected via the 50-pin (25x2 IDE) connector. Power inputs are connected either through the 4 pin power pins on the 4x1 portion of the IDE connector, or using the power pins located on the IDE 25x2 communications connector.

This section details the pin assignments for communication and power interfaces.

⚠	**Caution**
	• If the reserved pins are used for any purpose, compatibility with future versions of the SKB module can be compromised.

Note: The power pins for implementation of power on the IDE 25x2 connector should also be included if that powering method is selected as most appropriate for the application. See the power pin assignment section.

Table 1: Pin Assignment: RS485 Serial Interface (on 25x2 IDE connector)

PIN	SIGNAL	DESCRIPTION
39	RXTX-	Transmit/receive data negative side (A)
40	RXTX+	Transmit/receive data positive side (B)
42	485 Shield	RS485 signal shield
43	Trigger	Active low trigger signal, TTL multi-dropped, pulled UP at slave with 100K
44	Attention	Active low attention signal, open collector, pulled UP at master with 470 Ohms

Table 2: Pin Assignment: Simplex (SK/SP Emulation) Parallel Interface (on 25x2 IDE connector)

PIN	SIGNAL	DESCRIPTION
13	GND[1]	Shield
14	DGND[2]	Digital ground, **RESERVED FOR SK/SP EMULATION/ Power on 2x25**
15	BUSY	Busy output: low=idle, high= switching
16	D0	Data line 0
17	ERROR	Simplex (SK/SP emulation) Mode: reset error output low = normal, high = switch mechanism position check failed (channel position is verified when SK switch is reset) Enhanced Parallel Mode: ERROR asserted indicates an error code in the SKB error queue
18	D1	Data line 1
19	GND[1]	Shield
20	D2	Data line 2
21	GND[1]	Shield
22	D3	Data line 3
23	GND[1]	Shield
24	D4	Data line 4

Table 2: Pin Assignment: Simplex (SK/SP Emulation) Parallel Interface (on 25x2 IDE connector) (Continued)

25	/STROBE	/STROBE input, active low: a high to low pulse = read data lines; a high = ignore state of data lines. This line is internally pulled high via 10 K ohm resistor to 5 VDC. For the SK emulation the home line is also read in via the STROBE signal
26	D5	Data line 5
27	GND[1]	Shield
28	D6	Data line 6
29	GND[1]	Shield
30	/HOME	Home input: low sends the switch to the home position in Simplex (SK emulation) mode (i.e. this acts the same as the /RESET line defined in the SK/SP manual when the unit is wired as per this table)
31	GND[1]	Shield
32	DGND[2]	Digital ground, **RESERVED FOR SK/SP EMULATION/ Power on 2x25**
33	+5 VDC[2]	RESERVED FOR SK/SP EMULATION/ Power on 2x25
34	D7	Data line 7
35	+5 VDC[2]	RESERVED FOR SK/SP EMULATION/ Power on 2x25
36	+5 VDC[2]	RESERVED FOR SK/SP EMULATION/ Power on 2x25
37	NC	No connect
38	NC	No connect

1.   The GND (shield) signal lines should be connected to the common ground.
2.   The power pins are allocated on the assumption of Simplex operation for SK/SP emulation purposes. These pins should not be used if the user elects to power the unit using the 4x1 power connector.

Table 3: Pin Assignment: Enhanced Parallel Interface (on 25x2 IDE connector)

PIN	SIGNAL	DESCRIPTION
1-8	NC	No connect
9	/SOP	Start of packet
10	R/W	Read/write
11	/RESET	This is a micro controller unit (MCU) reset
12	RESERVED	For internal use only
13	GND[1]	Shield
14	DGND[2]	Digital ground, **RESERVED FOR SK/SP EMULATION/ Power on 2x25**
15	BUSY	Busy output: low=idle, high= switching
16	D0	Data line 0

Table 3: Pin Assignment: Enhanced Parallel Interface (on 25x2 IDE connector) (Continued)

17	ERROR	Simplex (SK/SP Emulation) Mode: reset error output low = normal, high = switch mechanism position check failed (channel position is verified when SK switch is reset) Enhanced Parallel Mode: ERROR asserted indicates an error code in the SKB error queue
18	D1	Data line 1
19	GND[1]	Shield
20	D2	Data line 2
21	GND[1]	Shield
22	D3	Data line 3
23	GND[1]	Shield
24	D4	Data line 4
25	/STROBE	/STROBE input, active low: a high to low pulse = read data lines; a high = ignore state of data lines. This line is internally pulled high via 10 K ohm resistor to 5 VDC. For the SK emulation the home line is also read in via the STROBE signal
26	D5	Data line 5
27	GND[1]	Shield
28	D6	Data line 6
29	GND[1]	Shield
30	/HOME	Home input: low sends the switch to the home position in Simplex (SK/SP emulation) mode (Replaces RESET line in emulation mode)
31	GND[1]	Shield
32	DGND[2]	Digital ground, **RESERVED FOR SK/SP EMULATION/ Power on 2x25**
33	+5 VDC[2]	RESERVED FOR SK/SP EMULATION/ Power on 2x25
34	D7	Data line 7
35	+5 VDC[2]	RESERVED FOR SK/SP EMULATION/ Power on 2x25
36	+5 VDC[2]	RESERVED FOR SK/SP EMULATION/ Power on 2x25
37	NC	No connect
38	NC	No connect
39	RXTX-	Transmit/receive data negative side (A)
40	RXTX+	Transmit/receive data positive side (B)
41	Bus Enable	Active high parallel bus enabler
42	485 Shield	RS485 signal shield
43	Trigger	Active low trigger signal, TTL multi-dropped, pulled UP at slave with 100K

Table 3: Pin Assignment: Enhanced Parallel Interface (on 25x2 IDE connector) (Continued)

44	Attention	Active low attention signal, open collector, pulled UP at master with 470 Ohms
45-50	NC	No connect

1. The GND (shield) signal lines should be connected to the common ground.
2. The pins should not be used during SKB operation, unless the power pins (listed in the table below) are NOT connected.

Table 4: Pin Assignment: Power using the 4x1 Power Connector

PIN	SIGNAL	DESCRIPTION
1	NC	No connect
2	DGND	Digital ground
3	NC	No connect
4	+5V DC	+5 VDC power input

Table 5: Pin Assignment: Power using the Power Pins on the 25x2 IDE Connector

PIN	SIGNAL	DESCRIPTION
13	GND	Shield
14	DGND	Digital ground, **RESERVED FOR SK EMULATION/ Power on 2x25**
31	GND	Shield
32	DGND	Digital ground, **RESERVED FOR SK EMULATION/ Power on 2x25**
33	+5 VDC	RESERVED FOR SK EMULATION/ Power on 2x25
35	+5 VDC	RESERVED FOR SK EMULATION/ Power on 2x25
36	+5 VDC	RESERVED FOR SK EMULATION/ Power on 2x25

Operation and Control Instructions

Note: PLEASE READ THIS SECTION VERY CAREFULLY IN ORDER TO UNDER-STAND THE VARIOUS METHODS BY WHICH THE SKB PRODUCT MAY BE CON-TROLLED.

In order to support the various implementation methods demanded by the OEM market, the SKB Series Fiberoptic Switch Module offers various control and power interfaces. All interfaces mentionned in this document are present on all units.

As the SKB product can be used as a subsystem, it is expected that the customer system engineer will make the decision concerning the appropriate type of implementation. Please contact JDS Uniphase Corp. if assistance is required in deciding which implementation method is best for your system.

As a guide, the following information provides a very brief introduction to each interface, and a sampling of applications favoring the interfaces identified.

The RS485 serial interface is located on the IDE 2x25 connector.

Examples of system level reasons for leveraging the RS485 serial interface are as follows:

- Multiple SKB units are required on the bus (takes advantage of addressing feature).
- The SKB unit is located a long way from the control and/or a noisy system (takes advantage of noise immunity of differential signal).
- The existing system bus is RS485 and/or in-house knowledge of the interface.

The parallel interfaces are also located on the IDE 2x25 connector. Two modes of implementation (Simplex and Enhanced) are offered with the tradeoff being functionality versus complexity of implementation. The Simplex parallel interface is unidirectional where data is presented and strobed in, and the Enhanced parallel interface is bi-directional, packet based.

Examples of system level reasons for leveraging the Simplex (SK/SP Emulation) parallel interface are as follows:

- The customer wishes to use this product to upgrade from the existing SK/SP product without any software or hardware changes (in order to take advantage of environmental enhancements).
- When the enhanced features are deemed 'not required' for the product being developed.

Examples of system level reasons for leveraging the Enhanced parallel interface are as follows:

- Reconfiguration or querying (status/health, identification, configuration) of the unit is deemed a requirement.
- Multiple SKB units are required on a parallel bus (can set up to 8 units in parallel using external address decoding and the Bus Enable line of the SKB).

Note: Situations may also arise where both parallel interfaces may be utilized by a customer at different stages of the procurement, manufacturing, sales, and support cycle. For instance, the implementation in the product may be in Simplex Mode but Incoming inspection, Manufacturing, and field technicians may use the Enhanced Mode (i.e. to take advantage of identification queries, configuration queries, status queries, and reconfiguration commands).

For the SKB product, power may be applied by two methods. It may be applied to the 4x1 Power Connector, **OR** it may be applied on the Power Pins of the IDE 2x25 Connector. The method of implementation will be determined by the customer system design requirements.

Examples of system level requirements for using the Power Connector (4x1):

- The SKB is located at a significant distance from the supply and/or temperature extremes are expected, hence heavier gauge wiring is required to ensure an adequate voltage level at the SKB unit.
- When harnessing multiple SKB units to a common supply.

Examples of system level requirements for using the power pins on the IDE 2x25 connector:

- Ease of assembly during manufacturing where a flat cable (generally 50 pin) is used (see note 1).
- Implementation in Simplex (SK/SP Emulation) Mode where a 26 pin flat cable (like the SK/SP product) is used (see note 1).
- When mounting the SBK product on a PCB.

Connecting Power

	Caution
⚠	- Protection against reverse connection of the power input is not incorporated in the SKB switch. Reverse connection of the power input results in damage to the switch. - The SKB switch requires that the power input be within the tolerance given at the unit. Care needs to be exercised in the design of the system power to compensate for any wiring losses in cabling. Failure to maintain the correct supply voltage can result in unpredictable operation of the switch.

When designing the system, it is important to note that:

1. The +5VDC required by the SKB switch is to be measured at the connector of the SKB unit itself, not the power source. This is particularly important when the SKB is expected to operate over a wide temperature range or is located at a distance from the power source (i.e. applications where system conditions are such that the voltage drop over the harness might exceed the SKB switch specifications).

2. Only one of the two means of power connection should be employed at one time.

Architecture Overview of the RS485 Serial and Enhanced Parallel Interfaces

On the RS485 Serial and Enhanced parallel interfaces, instructions and queries are received by the SKB module as command packets. Command packets describe a method of encapsulating a command opcode, a length code, and applicable parameter data in a format that can be interpreted by the SKB.

Command Packet Format

Multi-byte communication with the SKB module, via the RS485 Serial and Enhanced Parallel interfaces, is accomplished via command packets.

A standard command packet can be up to 255 bytes in length.

The first byte is always an opcode, which can be any number between 0 and 127. The most significant bit (MSB) is never set in a command packet opcode.

The second byte is always the length, in bytes, of the following parameter data. The value of the length byte corresponds to the number of bytes in the parameter data section of the command packet, regardless of the actual data type represented by the binary parameter data.

The minimum length of a command packet is two bytes. The opcode and length (even if zero) must be transmitted to the SKB module.

Command packets appear as follows:

OP	LEN	DATA

where OP = opcode and LEN = length.

The communication architecture of the SKB switch does not implement a command-response scheme. Each command packet sent is not necessarily answered with a response packet. Only those opcodes that represent a query generate a response packet.

Response Packet Format

Response packets refer to packets transmitted by the SKB switch for the purposes of returning query data. Response packets have an identical format as a standard command packet, with the MSB of the opcode byte set.

If, for example, an opcode of 0x01h was sent to the SKB switch and this opcode represented a query, the response packet would have an opcode of 0x81h.

The length byte of a response packet represents the total length of the parameter response data, regardless of the actual data types embedded in the parameter area.

Parameter Data Types

Parameter data of the command packet is limited to 253 bytes, which can be allocated at the discretion of the application according to standard data types shown in Table 6.

Table 6: Parameter Data Types

Data Type	Size in Bytes (Bits)
signed char	1 (8)
unsigned char	1 (8)
signed int	2 (16)
unsigned int	2 (16)
signed long	4 (32)
unsigned long	4 (32)
float	4 (32)

Byte Order

When utilizing data types larger than one byte, the byte order follows "little-endian" convention: the low-order byte (which holds the least significant bit, or LSB) is referenced as byte 0. Subsequent bytes progress toward the high-order byte (which holds the MSB). This sequence is illustrated as follows.

Single-byte bit order:

Bit	7	6	5	4	3	2	1	0

Double-byte bit order:

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Byte 0 (low)								Byte 1 (high)							

Quadruple-byte bit order:

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Byte 0 (low)								Byte 1							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Byte 2								Byte 3 (high)							

Example:

The 16-bit number represented by 0x1234h is split into two bytes as follows: 0x34h (Byte 0) and 0x12h (Byte 1). In the command or response packet, however, these bytes are contiguous and therefore appear as 0x3412h.

Operation and Control using the RS485 Serial Interface

The RS485 interface is a two wire differential bus used to communicate serially with the master device. The SKB RS485 interface operates over a range of 2400 to 4800 baud. The default baud rate for the switch is 2400 baud asynchronous, self-clocking.

The RS485 communication settings are:

- Eight data bits
- One stop bit
- No parity bits
- 2400 (default) and 4800 baud rate

Simultaneous operation of serial and parallel interface is not supported.

Connecting Multiple Switches using the RS485 Interface

Up to 31 RS485 unit loads can be connected to the differential bus. Therefore up to 30 SKB switches and one master controller can be used to construct an RS485 network. Exceeding the limit of 31 devices excessively loads the RS485 drivers and attenuates the differential signal. The consequence is reduced noise immunity of the bus and an increased error rate. Operation of more than 30 SKB's with a single master is not recommended nor guaranteed.

The most appropriate method of connecting RS485 nodes is by multidropping the connection from master to node 1, to node 2, and onward to node n. The bus must form a single continuous path.

Placing individual nodes at the end of long branches or spokes from the middle of the bus should be avoided. If branches are used, make them short. The preferred bus architecture is shown in Figure 5.
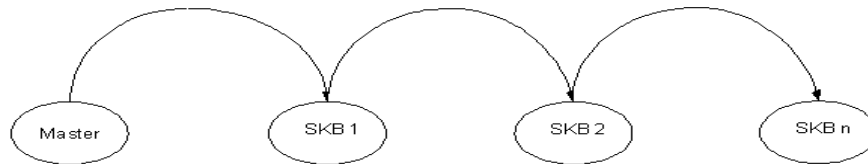
Figure 5: Preferred RS485 Bus Architecture

RS485 buses usually require line termination when fast transmissions, high data rates, or long cables lengths are employed. Although no termination is required if the bus cable length is short and transmission speed is low, it is always recommended.

Terminate bus lines at both ends of the main cable to prevent signal reflection. For example, in Figure 5, termination is applied at the Master node and SKB n node.

The common method of termination is parallel line termination, whereby a resistor is placed across the differential lines at the most extreme end of the bus (SKB n+1). The resistor value must be equal to the characteristic impedance of the cable. In practice, the resistor value needs to be slightly higher than characteristic impedance. A common mistake is to connect a terminating resistor at each node in the RS485 bus. This action causes line problems when more than four nodes are connected because the active bus driver is loaded excessively.

The maximum cable length specified for RS485 buses is 1219 meters (4000 feet). Generally, the longer the cable length, the slower the data transmission rate. All applicable data baud rates used by the SKB switch operate over the maximum cable length when proper termination is used and the number of nodes does not exceed 31.

Addressing using the RS485 Serial Interface

The addresses are outlined in Table 7.

Table 7: RS485 Addresses

Address	Description
0	Reserved for master. Cannot be an SKB switch.
2 to 31	Valid address range for SKB devices.
255	Broadcast address. Packets sent with a broadcast address are received and parsed by all active SKB devices on the RS485 bus.

Each SKB switch is pre-assigned an address of 1. If an SKB device is reset (either hard or soft), and the network address is 1, the ATTN line is asserted. The ATTN line is de-asserted when the device address is changed to something other than 1. This feature acts as a mechanism for informing the bus master that a device with the default address is connected to the bus. See the Application Note section for details regarding implementation of the Attention (ATTN) line.

Protocol for the RS485 Serial Interface

A proprietary link-layer RS485 protocol has been developed that enables network-based communication utilizing a single master and multiple slaves on a common bus. The protocol provides a high-level flow control mechanism (using acknowledge packets) and link-layer error detection (using CRC

packet validation). The RS485 protocol consists of two elements: the RS-485 link-layer communication packet and the master-slave acknowledge cycle.

The RS485 packet is composed of a number of bytes surrounding a data payload (Figure 6). The data payload section of the RS485 packet holds exactly one standard command packet, as illustrated. The packet bytes are designated as shown in Table 8.
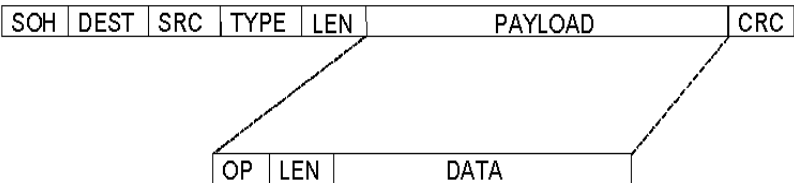
Figure 6: RS485 Link-Layer Packet and Command Packet

Table 8: RS485 Link-Layer Packet Fields

Packet Byte	Size (bits)	Description
SOH	8	Start of header byte (0x81)
DEST	8	Destination address of the packet (0x00 reserved for master, 0xFF reserved for broadcast)
SRC	8	Source address (for sending ACK's and responses)
TYPE	8	Packet type (DATA = 0, ACK = 1)
LEN	16	Length of payload section of the RS485 packet
CRC	16	16-bit CRC value with 0x1021 as polynomial

The master-slave acknowledge cycle refers the process of indicating to the sender that an RS485 packet has been received intact and that more packets can be sent. This action is accomplished by sending an RS485 ACK packet back to the sender. Once a valid RS485 packet is received, and the CRC has been verified, another packet can be sent by the master. Therefore, successful reception of the link-layer packet must be followed by an ACK response from the slave. If no ACK packet is received following transmission of a data packet with a specified timeout period, the sender needs to re-transmit the data packet. An ACK packet consists of a standard RS485 packet without a length byte, any data payload bytes, or CRC bytes. The type byte is defined as an ACK (1). The ACK packet is shown in Figure 7.
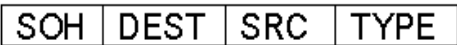
Figure 7: RS485 ACK Packet

This ACK cycle is reversed when response data packets are sent from the SKB slave to the master. In this case, the master is expected to acknowledge receipt of the link-layer packet by sending an ACK packet back to the slave.

A timeout period of 500 ms is used by the SKB switch for all serial data transfers. Therefore the time between subsequent bytes of a packet, or the time between data and ACK packets (being both sent and received, is 500 ms.

A holdoff period of 1 ms is observed by the SKB switch when transmitting data or ACK packets back to the master. The holdoff is a short delay to allow the master to prepare to receive data from the slave.

If a communication error occurs (for example, CRC mismatch), no ACK packet is transmitted to the sender.

If no ACK packet is received within a particular period following transmission of the last RS485 packet byte, retransmit the original RS485 packet.

Typical protocol is shown in Figure 8.
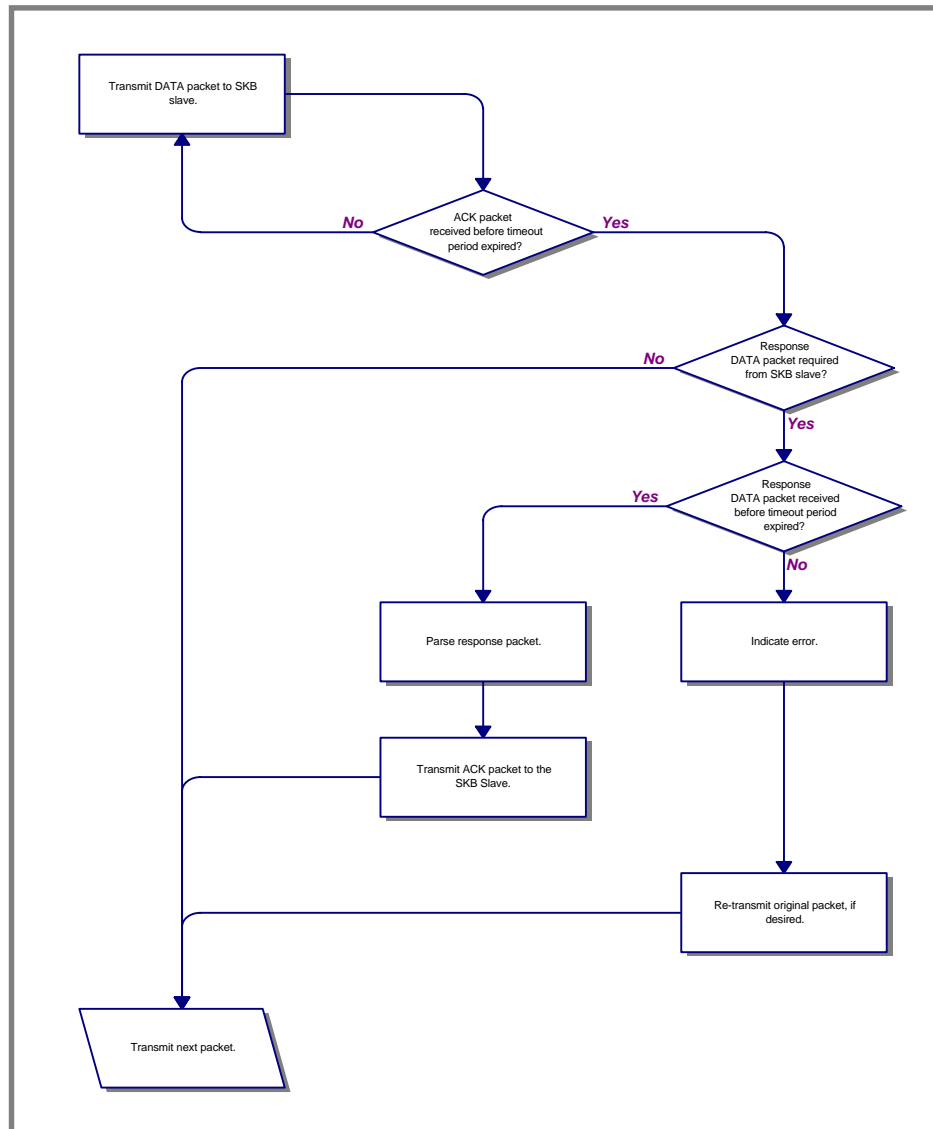
Figure 8: RS485 Network Implementation

Operation and Control using the Simplex Parallel Interface (SK/SP Emulation Mode)

The Simplex Parallel Interface (Emulation Mode)

The Simplex parallel interface is fully backwards compatible to the interface used on the SK/SP Series Fiberoptic switch. It also provides a simple interface when the advanced features of the SKB are not required.

The interface permits channel numbers to be strobed in using the STROBE line. As a reference for SK/SP users, the typical method of interface to a host controller for the SK/SP Series Fiberoptic Switch is shown below for reference.
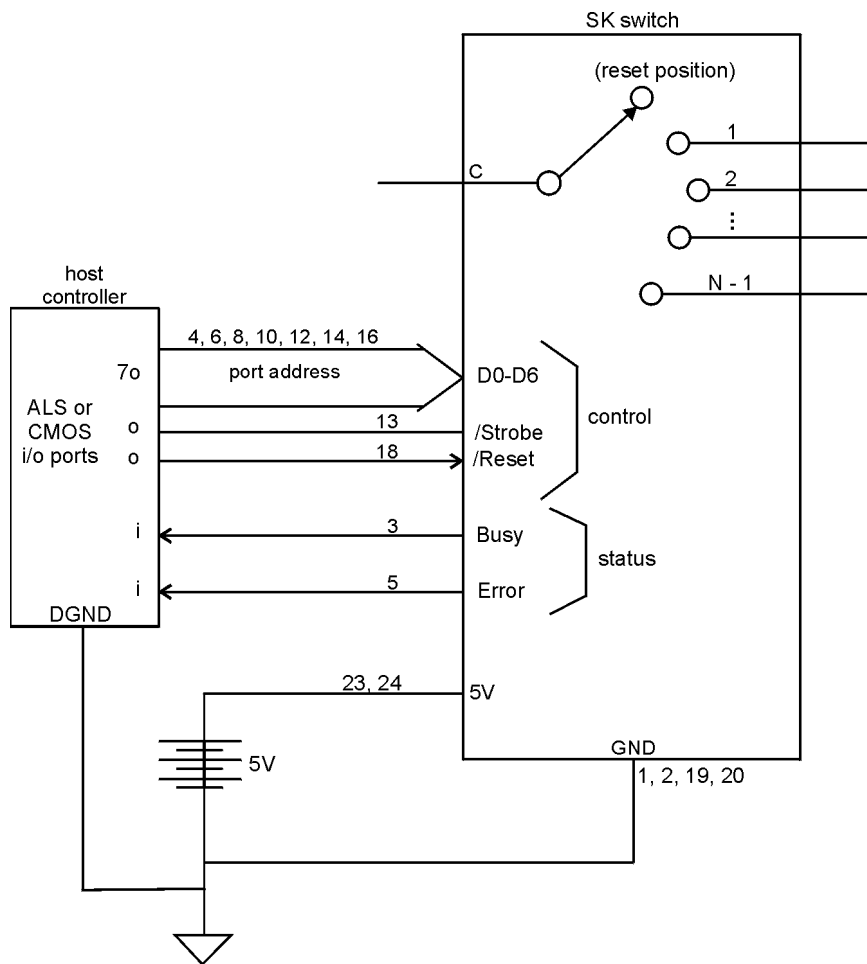
Figure 9: Typical Controller Connections

Simultaneous operation of serial and parallel interface is not supported.

Simplex Parallel Interface: Pin Functional Description

Data Lines (D0 to D6)

Valid channel numbers are strobed in through the data lines on high-to-low transitions of the /Strobe line. When a new channel is strobed in, the SK switch immediately selects the channel. The channel

number is represented as a binary number present on the data lines having the values listed in the channel address in Table 9.

Table 9: Channel Address Table

/Reset	D6	D5	D4	D3	D2	D1	D0	channel #
0								0 (reset)
1	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	1	2
1	0	0	0	0	0	1	0	3
1	0	0	0	0	0	1	1	4
1	0	0	0	0	1	0	0	5
1	0	0	0	0	1	0	1	6
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	0	0	1	0	1	1	1	24
1	0	0	1	1	0	0	0	25

The value 0 indicates that the input is set low (for example, <0.8 V DC); the value 1 indicates that the input is set high. For example, to select channel 9, D3 must be set high and the rest of the data lines must be set low.

/Reset Input Line

The /Reset line overrides the data lines. A low setting on this line forces the SK switch to go to the reset position and verify the previous channel position. /Reset must be strobed in using the /Strobe line. Changes on the /Reset line have no effect until a high-to-low transition occurs on the /Strobe line.

/Strobe Input Line

The /Strobe line strobes in the data on the data lines to select new channel positions. A change on the data lines has no effect until there is a high-to-low transition on the /Strobe line. The /Reset line also has no effect unless it is held low while the /Strobe line has a high-to-low transition.

Busy Output Line

The Busy line provides an indication of the switching mechanism state. The line is low when the switch is idle and high when the switching mechanism is moving to another port.

Error Output Line

The Error line reports the result of the self-test operation that occurs whenever the SK switch is reset. If the test fails, the Error line goes high and stays high until a self-test operation is evoked again (assuming the self-test passes on the next attempt). The error most often indicates a mechanical fault. For more information, contact JDS Uniphase.

Timing

When a channel address is strobed in from the data lines, the reset command is strobed in from the /Reset line. The Error line goes high if the reset function cannot verify the position of the switching mechanism (Figure 10).
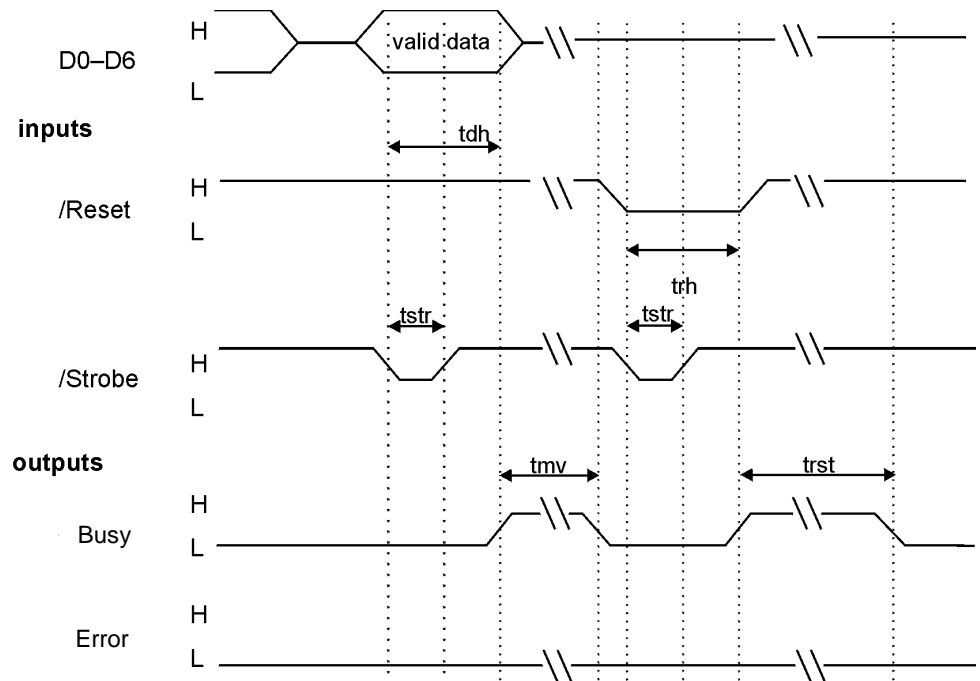
Figure 10: Timing Diagram

Timing Key

The timing key symbols and values are listed in Table 10.

Table 10: Timing Key

Symbol	Minimum	Maximum
tdh, data hold time	20 µs	–
tstr, strobe pulse width	1 µs	–
tmv, switching cycle time	–	0.55 ms
trh, reset hold time	20 µs	–
trst, reset cycle time	–	1.1 s

Operation and Control using the Enhanced Parallel Interface

Enhanced Parallel Interface

The Enhanced Parallel interface is similar to the RS485 Serial interface, as all instructions received by the switch are command packets containing a command opcode, a length code, and parameters.

> **Note:**   Since the command packet structure is the same as for the RS485 Serial Interface, the sections under RS485 that deal with Command Packet Format, Response Packet Format, Parameter Data Types, and Byte Order also apply to the Enhanced Parallel Interface

Enhanced Parallel Interface Voltage Levels

All parallel interface signals are TTL compatible. The active state of each signal is outlined in Table 11.

Table 11: Enhanced Parallel Interface States

Signal Name	Active State	Inactive State
D0 - D7	high	low
/STROBE	low	high
BUSY	high	low
ERROR	high	low
/SOP	low	high
R/W	high = read low = write	N/A
/RESET	low	high

Enhanced Parallel Timing

The SKB switch uses bidirectional parallel lines for the data bus (D0 to D7) and dedicated input/output lines for flow control. Data flow control is implemented on a byte-by-byte basis, using the BUSY output line of the SKB switch as the primary mechanism of controlling the data transfer rate. By using control signals, the actual signal timing can vary (within defined tolerances) according to the availability of the SKB switch, which is indicated with a low-level BUSY signal.

The primary control signals of the master are the /SOP and /STROBE lines. Transitions of the /SOP line are used to delimit the beginning and end of packets. The /STROBE line is used to signal the SKB switch to either read bytes from the data lines or write bytes to the data lines.

Timing dependencies are minimized, allowing use of control signals to regulate communication. However, the following timing requirements must be observed:

• A hold time of 5 µs must be applied when toggling SKB input lines (for example, R/W, D0-D7, /SOP, /STROBE, /RESET).
• The maximum period between sequential bytes (indicated by transitions of the /STROBE line) is 500 ms.

The following general rules apply:

- The master needs to ensure that the BUSY line is de-asserted (low) before toggling any parallel communication lines (for example, /SOP, /STROBE, and so on).
- Communication lines must be toggled according to the steps indicated in the protocol flow charts for read and write operations. Poll the error line following each operation.

Enhanced Parallel Interface Line Descriptions

Data Lines (D0...D7)

Byte data is composed of a binary eight-bit pattern presented on the /D0 to /D7 data lines. Input and output byte data are presented the same way.

The value 0 indicates that the input needs to be set low (for example, <0.8 V DC).

The value 1 indicates that the input needs to be set high (for example, ≥2 V DC).

/SOP Input Line

The /SOP line provides a data packet start/stop mechanism. Transition of the /SOP line from a high-to-low state indicates the beginning of a data packet, and all subsequent bytes placed on the data lines are considered packet data bytes. Transition of the /SOP line back from a low-to-high state indicates the end of a data packet. **The busy signal MUST drop before the /SOP command is withdrawn, or the communication sequence will be aborted**. The master is responsible for controlling the /SOP line.

/STROBE Input Line

The /STROBE line is used to signal the SKB switch to read data from or write data to the data lines. A change on the data lines has no effect until there is a high-to-low transition on the /STROBE line. The /STROBE line is driven by the master for both transmit and receive operations.

R/W Input Line

The R/W line is driven by the master as a bus control mechanism. When the R/W line is driven low, /D0-/D7, /SOP, and /STROBE line transitions are interpreted as input operations from the master to the slave. When R/W is driven high, operations are interpreted as output from the slave to the master.

BUSY Output Line

The BUSY line provides a flow control mechanism. The BUSY line is pulled high by the slave after each byte is transferred. The master does not toggle any lines until a high-to-low transition of the BUSY line is detected.

ERROR Output Line

The ERROR line is used to flag the master when the slave detects an error. When the error line is high, there is an error in the error queue. The ERROR line is driven low when the errors are read out of the error queue or the error queue is cleared.

/RESET

Reset resets the micro-controller unit (MCU) in the switch. All communication interfaces are reset.

Protocol for the Enhanced Parallel Interface

The read and write cycles follow a mechanism that tightly couples the control signals (SOP and STROBE lines on the master side and BUSY line on the slave side) to provide flow control. These cycles are defined as follows.

Read Cycle

The read cycle refers to the bus master reading bytes from the SKB slave (Figure 11). In this mode, the master ensures that the R/W line is pulled high. The master then toggles the /SOP line from the high to the low state, which signals the SKB switch to place the first data byte on the data lines. The BUSY line is held high to indicate to the master that a valid byte has been placed on the data lines. To indicate that the master has completed the read, the /STROBE line transitioned to low. The SKB switch subsequently pulls the BUSY line low to signal that the data acknowledgment has been received. The master then sets the STROBE to high. The BUSY transitions to high to indicate to the master when the next byte has been placed on the data lines. Upon completion of the last data byte transmission, the master resets the /SOP line from the low to the high state to indicate the end of the data packet.

Write Cycle

The write cycle refers to the bus master writing bytes to the SKB slave (Figure 12). In this mode, the master ensures that the R/W line is pulled low. The master then toggles the /SOP line from high to low, which indicates the beginning of a new packet. Binary byte data is subsequently placed on the data lines /D0 to /D7 and entered by use of the /STROBE line. After each STROBE, the BUSY line is held high until the SKB switch is ready to receive the next data byte. Upon completion of the last data byte transmission, the /SOP line is toggled from low to high, indicating the end of the data packet.

Please refer to the Application note section for details and examples of Enhanced parallel implementation.

Master   **Slave**
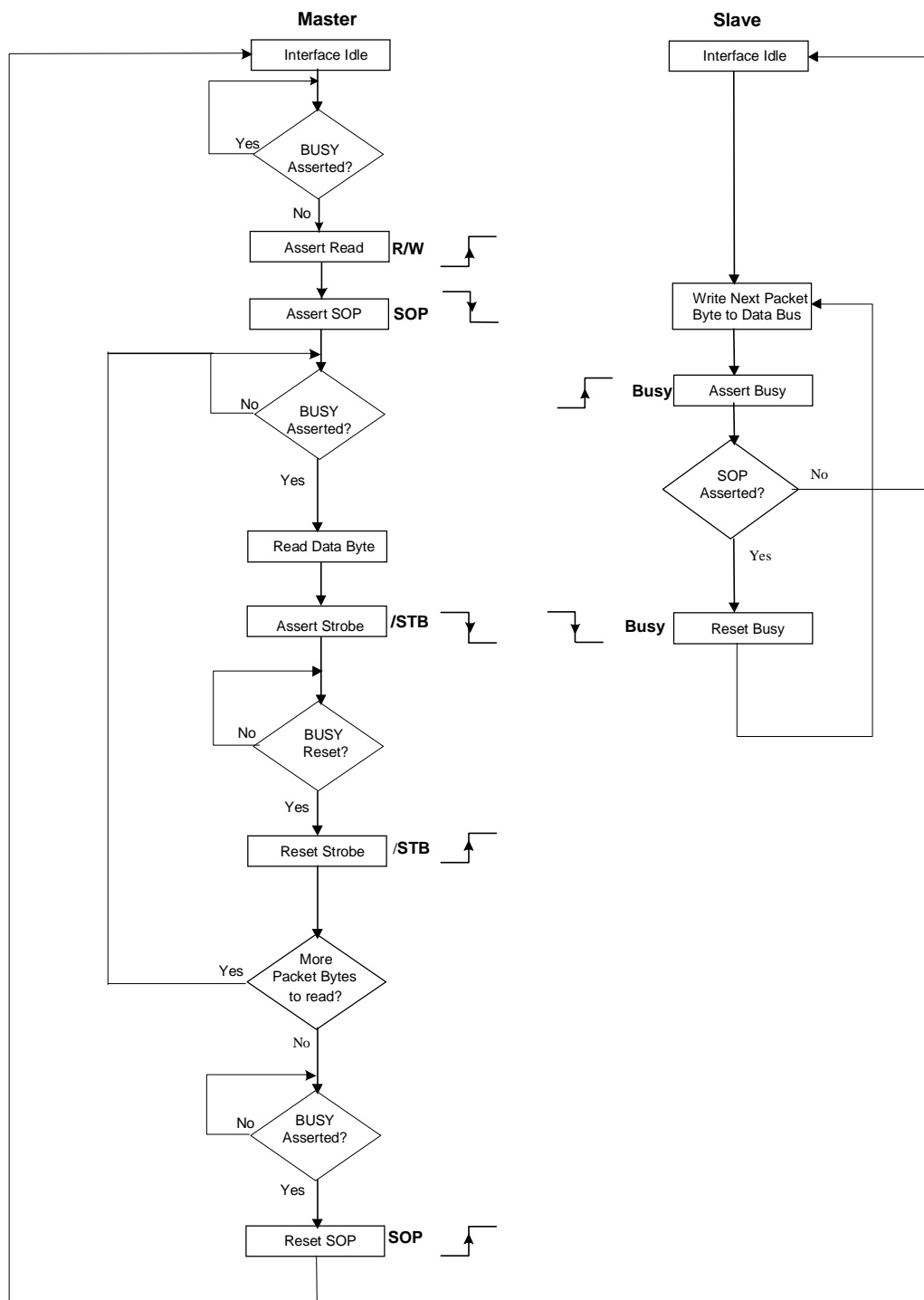
Figure 11: Flowchart of Read Cycle

Master

Slave

Interface Idle

BUSY Asserted?

Yes

No

Assert Write   **R/W**

Assert SOP   **SOP**

BUSY Asserted?

No

Yes

Set packet byte to bus

Assert Strobe   **/STB**

BUSY Reset?

No

Yes

Reset Strobe   **/STB**

BUSY Asserted?

No

Yes

More Packet Bytes to send?

Yes

No

Reset SOP   **SOP**

Interface Idle

Busy   Assert Busy

Read Packet Byte

Busy   Reset Busy

Save Packet Byte

Busy   Assert Busy

STROBE Asserted

Yes

No
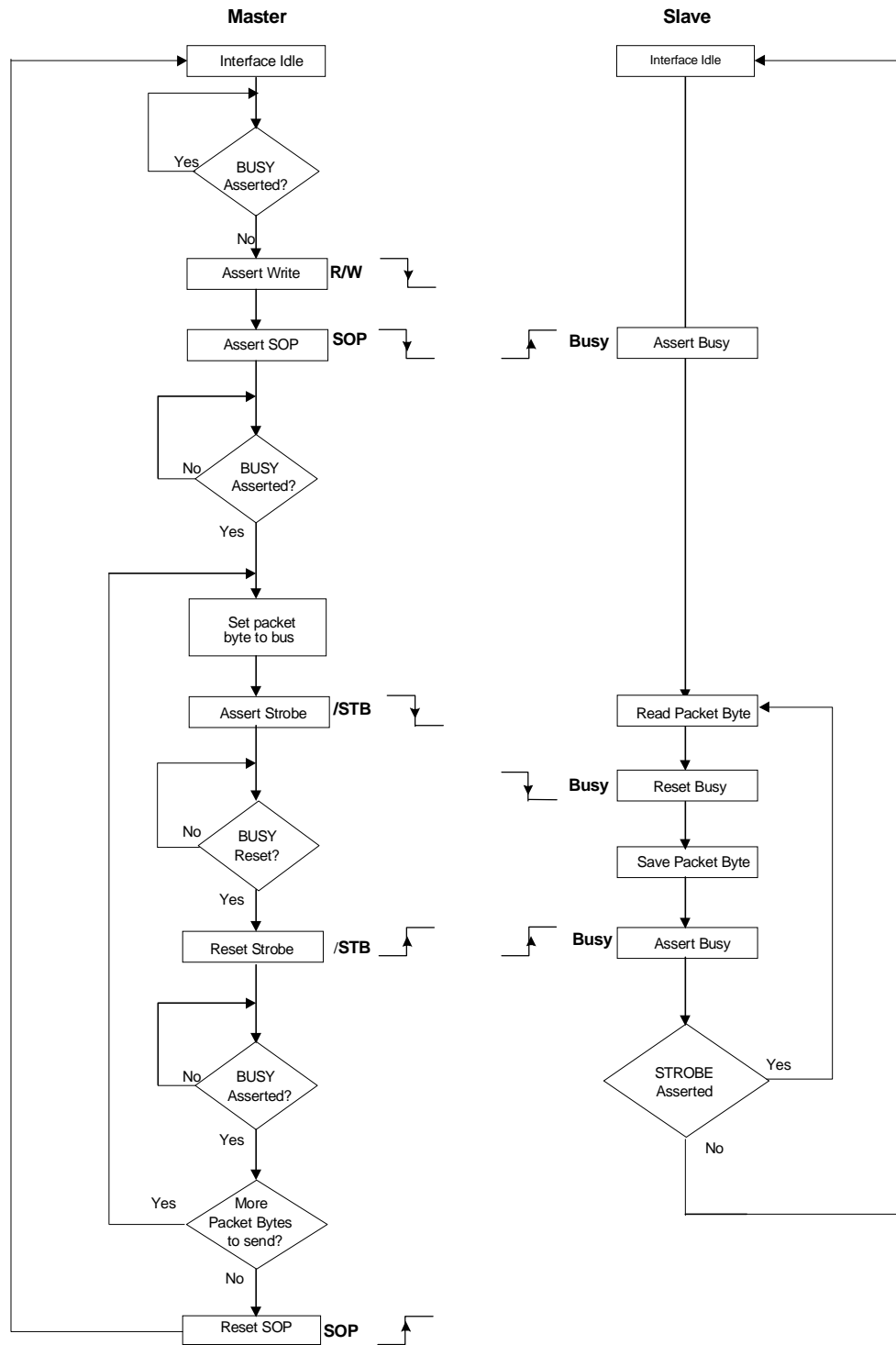
Figure 12: Flowchart of Write Cycle

Commands

The commands identified in the following sections apply to the Enhanced Parallel Interface and the RS485 Serial interface only.

Common Commands

SKB common commands refer to those operations and queries common to most switch modules and instruments. These commands represent the core functionality of the instrument module.

RESET

Description	Reset all switches to the default state. This command is functionally the same as a hardware Reset. The following major events occur: Current settings (channel positions are saved) A hardware reset is generated by the microcontroller On wakeup, non-latching switches move to the Reset position (factory default is a null-connect channel, but this can have been changed by the user), and latching switches stay on the same channel Also see the SWITCH command, which can be used to send individual switches to the reset position.
Parameters	NA
Parameter Description	NA

OPCODE	Length	Parameters
0x00	0x00	

IDN?

Description	Query identification information
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x01	0x00	

Response packet

OPCODE	Length	Parameters
0x81	0x22	U8 Serial_Num[15], U8 Model_Num[15], Core_Ver[2], App_Ver[2] Serial_Num (unsigned eight-bit array of 15 elements)--An array of 15 eight-bit integers (0 to 255) representing the serial number of the device. Unused bytes are zero-padded. Model_Num (unsigned eight-bit array of 15 elements)--An array of 15 eight-bit integers (0 to 255) representing the model number of the device. Unused bytes are zero-padded. Core_Ver (unsigned eight-bit array of two elements)--A pair of two eight-bit integers (0 to 255) representing the core firmware version. The first element corresponds to the major version and the second to the minor version (for example, 1.10). Unused bytes are zero-padded. App_Ver (unsigned eight-bit array of two elements)--A pair of two eight-bit integers (0 to 255) representing the application firmware version. The first element corresponds to the major version and the second to the minor version (for example, 1.10). Unused bytes are zero-padded. The numeric values of the bytes representing the serial, model, and version numbers are ASCII codes of equivalent character bytes. Therefore, U8 data can be directly translated into ASCII character data for display to the user.

STATUS?

Description	Query the status register value
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x02	0x00	

Response packet

OPCODE	Length	Parameters
0x82	0x01	U8 Status_reg Status_reg (unsigned eight-bit)--Current binary value of the Module Status Register (MSR), as indicated in the following table.

Bit	7	6	5	4	3	2	1	0
Function	ERR	EQO	ALRM	OPP				
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

ERR (ERROR, bit 7)--This bit indicates that an error code has been written to the error queue. It is cleared when the error queue is cleared. The light emitting diode produces a red light if this bit is set.

EQO (ERROR QUEUE OVERFLOW, bit 6)--This bit indicates that more than eight errors have occurred and the error queue has overflowed. It is cleared when the error queue is read at least once and can hold another error code.

ALRM (ALARM, bit 5)--This bit indicates that a bit in the alarm register is set. It is cleared when the alarm register is cleared. The light emitting diode produces an amber light if this bit is set.

OPP (OPERATION IN PROGRESS, bit 4)--This bit indicates that a critical operation is in process. It is cleared when the operation is complete.

> **Note:** In the absence of alarm or error condition, the light emitting diode stays green.In the presence of both these conditions, the light emitting diode reports the error condition by turning red.

ALARM?

Description	Query the alarm register value
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x03	0x00	

Response packet

OPCODE	Length	Parameters
0x83	0x02	U16 Alarm_reg Alarm_reg (unsigned 16-bit)--Current binary value of the Alarm Register (AR), as indicated in the following table

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	EPV	OT	UT	CFO												
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EPV (EEPROM VERIFY FAIL, bit 15)--This bit indicates that the verify operation of an EEPROM write failed. It is cleared when the AR is read.

OT (OVER TEMPERATURE, bit 14)--This bit indicates that ambient temperature of the module has exceeded the high temperature threshold for a period of at least 10 seconds. It is cleared when the temperature falls below the high temperature threshold.

UT (UNDER TEMPERATURE, bit 13)--This bit indicates that ambient temperature of the module has dropped below the low temperature threshold for a period of at least 10 seconds. It is cleared when the temperature falls below the high temperature threshold.

CFO (CONFIGURATION OVERFLOW, bit 12)--This bit indicates that user configuration commands have been executed more than 50,000 times. This bit is not cleared when the configuration command counter exceeds 50,000. This bit can only be cleared at the JDS Uniphase factory.

LERROR?

Description	Read and clear last error message in the error queue
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x04	0x00	

Response packet

OPCODE	Length	Parameters
0x84	0x01	U8 Error_code Error_Code (unsigned eight-bit)--Error code represents the last error that occurred, as indicated in the following table

Error Code	Description
0 (0x00)	No error--OK
1 (0x01)	Invalid command opcode
2 (0x02)	Command packet length mismatch
3 (0x03)	Invalid packet length
4 (0x04)	Invalid command packet parameter
5 (0x05)	EEPROM write failure
6 (0x06)	Switch 1 failure
7 (0x07)	Switch 2 failure
8 (0x08)	Switch 3 failure
9 (0x09)	Switch 4 failure
10 (0x0A)	Invalid spare channel
11 (0x0B)	Communication interface receive time-out
12 (0x0C)	Communication interface transmit time-out
13 (0x0D)	Communication packet invalid
14 (0x0E)	Communication receive run-on condition
15 (0x0F)	Communication transmit run-on condition
16 (0x10)	Communication invalid transmit operation initiated by master
17 (0x11)	Reserved
18 (0x12)	Communication invalid STROBE received
19 (0x13)	RS485 link-layer packet CRC mismatch
20 (0x14)	RS485 invalid link-layer packet length
21 (0x15)	RS485 invalid link-layer packet type
22 (0x16)	RS485 invalid source address
23 (0x17)	RS485 link-layer packet ACK transmit timeout
24 (0x18)	RS485 link-layer packet ACK receive timeout
25 (0x19)	RS485 link-layer ACK expected but DATA packet received
26 (0x1A)	RS485 unexpected ACK packet received
27 (0x1B)	UART overrun (bytes missed in serial receive)
28 (0x1C)	Undefined error

EQCLEAR

Command packet

Description	Erase all entries in the error queue
Parameters	NA
Parameter Description	NA

OPCODE	Length	Parameters
0x05	0x00	

TEMP?

Description	Query temperature information. All temperature information is referenced in degrees Kelvin.
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x06	0x00	

Response packet

OPCODE	Length	Parameters
0x86	0x06	U16 Hi_temp, U16 Low_temp, U16 Temp Hi_temp (unsigned 16-bit)--Configured high temperature threshold (234 – 358 °K) Low_temp (unsigned 16-bit)--Configured low temperature threshold (233 – 357 °K) Temp (unsigned 16-bit)--Actual ambient temperature (233 – 358 °K) Temperature (°C) = Temperature (°K) - 273 All temperature information is referenced in degrees Kelvin. Conversions are as follows: 1 °C = 1 °K and 0 °C = 273 °K approximately 1 °F = 0.55 °K and 0 °F = 255.37 °K

STIMER?

Description	Query the system timer. System time is defined from the last reset (includes power cycle and hard or soft reset)
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x0B	0x00	

Response packet

OPCODE	Length	Parameters
0x0B	0x07	U16 Msec, U8 Sec, U8 Min, U16 Hour, U8 Year

Msec (unsigned 16-bit)--The current millisecond timer index (0 to 999).

Sec (unsigned eight-bit)--The current second timer index (0 to 59).

Min (unsigned eight-bit)--The current minute timer index (0 to 59).

Hour (unsigned 16-bit)--The current hour timer index (0 to 8759).

Year (unsigned eight-bit)--The current year timer index (0 to 255).

The system timer is returned as seven bytes as described previously. These bytes can be extracted into a "C" structure, for example, as follows:

```
struct TIMER      /* define system timer struct */
{
  U16_t Msec;    /* milliseconds */
  U8_t Sec ;    /* seconds */
  U8_t Min ;    /* minutes */
  U16_t Hour;    /* hours */
  U8_t Year;    /* years (approx. 8760 hours) */
};
```

RESET_STIMER

Description	Reset the system timer to 0
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x0C	0x00	

SWITCH

Description	Modify switch state
Parameters	Switch, Input, Output
Parameter Description	Switch (unsigned eight-bit)--switch number Input (unsigned eight bit)--input channel Output (unsigned eight bit)--output channel

Command packet

OPCODE	Length	Parameters
0x20	0x03	U8 Switch, U8 Input, U8 Output Switch (unsigned eight-bit)--Logical switch number upon which to perform action (for example, 1 to 4) Input (unsigned eight-bit)--Input channel to connect (for example, 1 on a 1xN switch) Output (unsigned eight-bit)--Output channel to connect specified input channel, where 0 = reset position (factory configured to be a null connect, but this can have been changed by user) 1 to 200 = output channel number 254 = previous channel; ignored if the switch is on the first channel 255 = next channel; ignored if the switch is on the last channel

SWITCH?

Description	Query logical switch state
Parameters	Switch, Input
Parameter Description	Switch (unsigned eight-bit)--switch number Input (unsigned eight-bit)--input channel number

Command packet

OPCODE	Length	Parameters
0x21	0x02	U8 Switch, U8 Input Switch (unsigned eight-bit)--Logical switch number upon which to read information (for example, 1 to 4) Input (unsigned eight-bit)--Input channel to find connection of

Response packet

OPCODE	Length	Parameters
0xA1	0x01	U8 Output Output (unsigned eight-bit)--The output channel connected to the input channel specified

NUM_SWITCH?

Description	Query number of logical switches
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x22	0x00	

Response packet

OPCODE	Length	Parameters
0xA2	0x01	U8 Switches Switches (unsigned eight-bit)--The number of logical switches in the module (for example, 1 to 4)

LEARN?

Description	Query command(s) required to return the switch to current state following reset. This query returns the information required to send the switch back to the state it was in prior to reset.
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x24	0x00	

Response packet

OPCODE	Length	Parameters
0xA4	0x05 to 0x14[1]	(1-5) (U8 Opcode, U8 Len, U8 Sw_Id, U8 Cur_In, U8 Cur_Out) Opcode (unsigned eight-bit)--"SWITCH" command opcode (0x20) Sw_Id (unsigned eight-bit)--Switch number (1 to 4) Cur_In (unsigned eight-bit)--Current input channel of the switch (1 to 2) Cur_Out (unsigned eight-bit)--Current output channel of the switch (0 to 200)

1.   The length is variable, depending on the number of switches in the module.

TST?

Description	Perform a self-test operation and return results
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x25	0x00	

Response packet

OPCODE	Length	Parameters
0xA5	0x01 to 0x04[1]	U8 Sw1_Result, U8 Sw2_Result, U8 Sw3_Result, U8 Sw4_Result, Sw1_Result (unsigned eight-bit)--Self-test result (0/1, where 0 = pass and 1 = fail) Sw2_Result (unsigned eight-bit)--Self-test result (0/1, where 0 = pass and 1 = fail) (if necessary) Sw3_Result (unsigned eight-bit)--Self-test result (0/1, where 0 = pass and 1 = fail) (if necessary) Sw4_Result (unsigned eight-bit)--Self-test result (0/1, where 0 = pass and 1 = fail) (if necessary)

1.   The length is variable, depending on the number of switches in the module.

> **Note:**   The response time for the TST? Query can vary form 0.5 to 4 seconds.

SAVE

Description	Save the current state of all switches in the module for later recall at one of 10 locations
Parameters	Location
Parameter Description	Location (unsigned eight-bit)--Memory location to save state

Command packet

OPCODE	Length	Parameters
0x26	0x01	U8 Location Location (unsigned eight-bit)--Memory location of state data (0 to 9)

RECALL

Description	Recall a module state previously saved
Parameters	Location
Parameter Description	Location (unsigned eight bit)--memory location

Command packet

OPCODE	Length	Parameters
0x27	0x01	U8 Location Location (unsigned eight-bit)--Memory location of state data (0 to 9)

Configuration Commands

SKB configuration commands are operations and queries that allow users to modify basic instrument settings. These commands provide additional functionality than is available on current instrument modules.

CONFIG?

Description	Query the configuration of all logical switches
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x23	0x00	

Response packet

OPCODE	Length	Parameters
0xA3	0x04 to 0x0F[1]	(1-4) * (U8 Sw_Id, U8 Sw_Type, U8 Max_In, U8 Max_Out) Sw_Id (unsigned eight-bit)--Logical switch identification number (1 to 4) Sw_Type (unsigned eight-bit)--Physical switch type (0:motor or 1:relay) Max_In (unsigned eight-bit)--Maximum number of inputs of the switch (1 to 2) Max_Out (unsigned eight-bit)--Maximum number of outputs of the switch (1 to 200)

1. The length is variable, depending on the number of switches in the module.

HITEMP

Description	Set the upper temperature threshold
Parameters	Temp
Parameter Description	Temp (unsigned 16-bit)--The °K high temperature threshold that, if exceeded, causes the OT alarm register bit to be set

Command packet

OPCODE	Length	Parameters
0x07	0x02	U16 Hi_temp Hi_temp (unsigned 16-bit)--High temperature threshold (234 to 353 °K)

Note: All temperature information is referenced in degrees Kelvin. Conversions are as follows:
1 °C = 1 °K and 0 °C = 273 °K approximately
1 °F = 0.55 °K and 0 °F = 255.37 °K

LOWTEMP

Description	Set the lower temperature threshold
Parameters	Temp
Parameter Description	Temp (unsigned eight-bit)--The °K low temperature threshold that, if exceeded, causes the UT alarm register bit to be set

Command packet

OPCODE	Length	Parameters
0x08	0x02	U16 Low_temp Low_temp (unsigned 16-bit)--Low temperature threshold (233 to 352 °K)

Note: See note from the previous HITEMP section.

SPARES?

Description	Query the current number of spare fibers available on the logical switch specified
Parameters	Switch
Parameter Description	Switch (unsigned eight-bit)--logical switch

Command packet

OPCODE	Length	Parameters
0x30	0x01	U8 Switch Switch (unsigned eight-bit)--Logical switch number (1 to 4)

Response packet

OPCODE	Length	Parameters
0xB0	0x01	U8 Spares Spares (unsigned eight-bit)--The number of spare channels currently configured for the switch

REPLACE

Description	Replace output channel with factory spare
Parameters	Switch, Output, Spare
Parameter Description	Switch (unsigned eight-bit)--switch number Output (unsigned eight-bit)--channel number to be replaced Spare (unsigned eight-bit)--factory spare number

Command packet

OPCODE	Length	Parameters
0x33	0x3	U8 Switch, U8 Output, U8 Spare Switch (unsigned eight-bit)--Logical switch number (1 to 4) Output (unsigned eight-bit)--The replaced output channel (1 to 200) Spare (unsigned eight-bit)--The factory spare number used for the replacement (1 to 200) This command resets the switch.

SWAP_CHANNEL

Description	Swap channel designations between two optical fibers. This command can be used to reorder channels that have been swapped
Parameters	Switch, Output1, Output2
Parameter Description	Switch (unsigned eight-bit)--switch number Output1 (unsigned eight-bit)--first output channel Output2 (unsigned eight-bit)--second output channel

Command packet

OPCODE	Length	Parameters
0x34	0x03	U8 Switch, U8 Output1, U8 Output2 Switch (unsigned eight-bit)--Logical switch number (1 to 4) Output1 (unsigned eight-bit)--The first output channel (1 to 200) Output2 (unsigned eight-bit)--The second output channel (1 to 200) This command resets the switch.

LATCHING?

Description	Query latching status of the switch
Parameters	Switch
Parameter Description	Switch (unsigned eight-bit)--switch number

Command packet

OPCODE	Length	Parameters
0x35	0x01	U8 Switch Switch (unsigned eight-bit)--Logical switch number (1 to 4)

Response packet

OPCODE	Length	Parameters
0xB5	0x01	U8 Latching_Status Latching_Status (unsigned eight-bit)--The status of the switch (1 = latching, 0 = non-latching)

RESET_CHANNEL?

Description	Query output channel associated with the reset position for the selected switch
Parameters	Switch
Parameter Description	Switch (unsigned eight-bit)--switch number

Command packet

OPCODE	Length	Parameters
0x36	0x01	U8 Switch Switch (unsigned eight-bit)--Logical switch number (1 to 4)

Response packet

OPCODE	Length	Parameters
0xB6	0x01	U8 Output_Channel Output_Channel (unsigned eight-bit)--The output channel associated with the reset position (0 to 200)

RESET_CHANNEL

Description	Define the reset output channel
Parameters	Reset_Channel, Switch
Parameter Description	Reset_Channel (unsigned eight-bit)--Output channel number to be associated with the reset channel Switch (unsigned eight-bit)-- switch number

Command packet

OPCODE	Length	Parameters
0x37	0x02	U8 Switch, U8 Reset_Channel Switch (unsigned eight-bit)--Logical switch number (1-4) Reset_Channel (unsigned eight-bit)--The output channel to be associated with the reset position (0 to 200)

Note: The reset channel is defined in reference to input port 1.This command will cause the switch to be reset.

RECALL_FAC_SETTING

Description	Recall the original factory setting of the switch
Parameters	Switch
Parameter Description	Switch (unsigned eight-bit)--switch number

Command packet

OPCODE	Length	Parameters
0x38	0x01	U8 Switch Switch (unsigned eight-bit)--Logical switch number (1 to 4) This command resets the switch. The setting is modified with the MODIFY_SPEED, RESET_CHANNEL, REPLACE, and SWAP_CHANNEL commands. Commands are reset to factory defaults.

SPEED?

Description	Query the speed of the switch
Parameters	Switch
Parameter Description	Switch (unsigned eight-bit)--switch number

Command packet

OPCODE	Length	Parameters
0x39	0x01	U8 Switch Switch (unsigned eight-bit)--Logical switch number (1 to 4)

Response packet

OPCODE	Length	Parameters
0xB9	0x01	U8 Speed Speed (unsigned eight-bit)--The speed setting of the switch (1 to 5) The speed setting of the switch (1-5), where 1 is the slowest speed and 5 the fastest. Only speeds 1 and 5 are implemented

MODIFY_SPEED

Description	Modify the speed setting of the specified switch
Parameters	Switch, Speed
Parameter Description	Switch (unsigned eight-bit)--switch number Speed (unsigned eight-bit)--speed setting for specified switch

Command packet

OPCODE	Length	Parameters
0x3A	0x02	U8 Switch, U8 Speed Switch (unsigned eight-bit)--Logical switch number (1 to 4) Speed (unsigned eight-bit)--The speed setting of the switch (1 to 5) The speed setting of the switch (1-5), where 1 is the slowest speed and 5 the fastest. Only speeds 1 and 5 are implemented.

CONNECTION_TIME?

Description	Query the time to connect two channels, in ms. This test breaks the current connection. The SKB switch allows the user to confirm the specified time to switch between channels. The CONNECTION_TIME? query physically checks the time by switching between the start and destination channel and outputs the results from the internal clock.
Parameters	U8 Switch, U8 Start, U8 Destination
Parameter Description	Switch (unsigned eight-bit)--switch number Start (unsigned eight-bit)--output channel to begin measurement Destination (unsigned eight-bit)--destination output channel

Command packet

OPCODE	Length	Parameters
0x3B	0x03	U8 Switch, U8 Start, U8 Destination Switch (unsigned eight-bit)--Logical switch number (1 to 4) Start (unsigned eight bit)--The output channel of the specified switch where measurement begins Destination (unsigned eight-bit)--The destination output channel on the specified switch

Response packet

OPCODE	Length	Parameters
0xBB	0x02	U16 Interval Interval (unsigned 16-bit)--number in milliseconds

SET_DEVICE_ADDRESS

Description	Modify the RS485 network address of the switch
Parameters	Address
Parameter Description	Address (unsigned eight-bit)--network address

Command packet

OPCODE	Length	Parameters
0x3D	0x01	U8 Address Address (unsigned eight-bit)--Network address (1 to 31) NOTE: The module is factory configured with address unless specified other-wise. Address 0 reserved for master controller.

DEVICE_ADDRESS?

Description	Query the RS485 network address of the device
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x3E	0x00	

Response packet

OPCODE	Length	Parameters
0xBE	0x01	U8 Address Address (unsigned eight-bit)--Network address (1 to 31)

SET_TRIGGER_CMD

Description	Set the trigger command to be executed when the trigger line is asserted
Parameters	Opcode, Length, Param1, Param2, Param3
Parameter Description	Opcode (unsigned eight-bit)--opcode of command to be executed Length --the length of the data portion Param1, Param2, Param3 (unsigned eight-bits)--first, second, and third parameter of the selected command (number of parameters ranges from 0 to 3 depending of the selected command) Note that the default opcode is for reset (0x00

Command packet

OPCODE	Length	Parameters
0x3F	0x02 to 0x0A[1]	U8 Opcode, U8 Length, U8 Param1, U8 Param2, U8 Param3 Opcode (unsigned eight-bit)--Opcode of the command selected to be executed as part of the trigger command (0x20 to 0x27) Param1-Param8 (unsigned eight bit)--Data payload bytes specific to the opcode specified.

1.   The length is variable, depending on the selected command.

TRIGGER_CMD?

Description	Query the trigger command
Parameters	NA
Parameter Description	NA

Command packet

OPCODE	Length	Parameters
0x40	0x00	

Response packet

OPCODE	Length	Parameters
0xC0	0x02 to 0x0A[1]	U8 Opcode, U8 Length, U8 Param1--U8 Param8 Opcode (unsigned eight-bit)-- Opcode of the command selected to be executed as part of the trigger command (0x20 to 0x27) Length (unsigned eight bit)--The length of the data portion of the command packet. Param1 - Param8 (unsigned eight-bit)--Data payload bytes specific to the opcode specified

1.   The length is variable, depending on the selected command.

DEVICE_BAUD

Description	Modify the baud rate of the device
Parameters	Baud_Rate
Parameter Description	Baud_Rate - Baud rate code

Command packet

OPCODE	Length	Parameters
0x41	0x01	U8 Baud_Rate Baud_Rate (unsigned eight-bit)--Baud rate setting (0 - 4) defined as follows: 0 - 2400 baud 1 - 4800 baud

DEVICE_BAUD?

Description	Query the baud rate of the device
Parameters	NA
Parameter Description	NA

Command Packet

OPCODE	Length	Parameters
0x42	0x00	

Response Packet

OPCODE	Length	Parameters
0xC2	0x01	U8 Baud_Rate Baud_Rate (unsigned eight-bit)--Baud rate setting (0 - 4) defined as follows: 0 - 2400 baud 1 - 4800 baud

Application Notes

APPLICATION NOTE: Using the ATTENTION Output Line

The intent of this application note is to describe a typical application of the ATTENTION output line of the SKB interface.

The ATTNENTION (ATTN) line is intended to be used as a mechanism to easily add new devices to an RS-485 network of SKB switches.

The ATTN line is defined as pin 44 of the 2x25-pin HDD connector on an SKB switch.

An SKB device configured with a device address of 1 (the factory default address) will continuously assert the ATTN line. The ATTN line is active high.

The ATTN line is an open collector signal that is terminated at the *master end only* by a 470 Ohms resistor connected to V+. Upon connection of a terminating resistor, transitions of the line will be detectable to the master controller.

The ATTN line may be included as part of the network signal harness (or backplane) and connected to all devices, or may be connected to a single network drop and the master controller.

The operation of the ATTN line is intended to facilitate RS-485 network operation, as follows:

1. At start-up the master should perform a device query (ie. SWITCH or IDN query) through the entire RS-485 address range (ie. 1 – 31) to determine which addresses have active devices. This is determined by receipt of a valid response to the query. The master should build a list of used and unused RS-485 addresses.

2. A new SKB switch (with an address of 1) is added to the RS-485 network and powered-up. This will cause the ATTN to be asserted.

3. The master recognizes that the ATTN line is asserted, indicating that a device having address 1 has been added to the network.

4. The master assigns the next unused RS-485 address to the device at address 1 (ie SET_DEVICE_ADDRESS to next unused from the list built in step 1.). This will cause the ATTN signal to be de-asserted.

5. Additional devices can be added to the network one-by-one in the same fashion, staring at step 2.

6. If there are no unused RS-485 addresses, the SKB configured with address 1 remains at that address, and the ATTN line will remain asserted.

APPLICATION NOTE: Using the TRIGGER Input Line

The intent of this application note is to define details of the trigger line and to describe a typical application.

The SKB interface connector includes a TRIGGER line which can be used to execute a *trigger command*.

The *trigger command* is a standard command packet which is inserted into the command processor when the trigger line is asserted. The trigger line is asserted by pulling LOW, and the trigger com-

mand is executed on the high-to-low transition of the line. Therefore holding the line in a continuously asserted state will not cause repeated triggers.

The trigger command can be any valid SKB command, and is factory configured as RESET (opcode 0x00). Note that once a trigger command is defined, that command is persistent and not changed by a reset.

The primary intent of the trigger line is to provide the ability for the master controller to cause a group of SKB switches to execute a common function. This is typically achieved by integrating the trigger line with an RS-485 network harness.

Note that if a command packet is being received by the SKB switch via any of the communication interfaces, asserting the trigger line will interrupt the process and the bytes received will be discarded. The trigger command is executed in priority order, meaning that any commands currently executing will be allowed to complete.

Care should be taken when selecting a trigger command. For example, setting a trigger command to a query will cause the response packet to be discarded and not transmitted.

A typical use of the trigger line is as follows:

In an application where the devices connected to the switch outputs are sensitive to high power, the trigger command can be specified to connect the input to a specific channel which can tolerate high-power signals. This input is then monitored until the power is tolerable to other devices. In this application, the power of the input signal is constantly monitored and the trigger line is asserted if the power exceeds tolerable thresholds.

1. Set the trigger command to execute a SWITCH command to a channel which is intended to handle high-power input (ie. signal is attenuated after exiting the SKB switch).

2. Tap input channel monitor signal power.

3. During switching operations monitor the power of the incoming signal to ensure is with tolerance for the output channels being used.

4. If input power exceeds maximum thresholds for the output device, assert the trigger line to immediately cause the switch to connect the input to the high-power output channel.

5. Monitor the high-power channel until signal power returns to tolerable levels, and resume normal switching operations.

APPLICATION NOTE: Enhanced Parallel Communication Examples

The intent of this application note is to provide details of the SKB enhanced parallel communication interface. This includes examples of actual oscilloscope screen images captured during both high- and low-speed parallel operations.

Write Cycle

The write cycle refers to the bus master controller strobing bytes into the SKB slave. In this mode, the master ensures that the R/W line is low. The master then toggles the /SOP line from high to low, which indicates the beginning of a new packet. Binary byte data is subsequently placed on the data lines /D0 to /D7 and entered by use of the /STROBE line. The SKB slave utilizes the BUSY line to control the data flow.   Throughout the process, timing dependencies are eliminated by interlocking the /STROBE and BUSY lines. Upon completion of the last data byte transmission, the /SOP line is toggled from low to high, indicating the end of the data packet.

Figure 13 (high-speed master ~200 µs /STROBE pulse width) and Figure 14 (low-speed master -- ~18ms /STROBE pulse width) are oscilloscope trace captures showing typical line toggling for a master write cycle. These figures show the relationship between R/W, /SOP, and /STROBE input lines and the BUSY output line during a five-byte command packet write to the SKB. Note that in each scenario illustrated, the line toggling is identical and independent of the /STROBE pulse time. Figure 13 (high-speed master ~200 µs /STROBE pulse width) and Figure 14 (low-speed master -- ~18ms /STROBE pulse width) are oscilloscope trace captures showing typical line toggling for a master write cycle. These figures show the relationship between R/W, /SOP, and /STROBE input lines and the BUSY output line during a five-byte command packet write to the SKB. Note that in each scenario illustrated, the line toggling is identical and independent of the /STROBE pulse time.
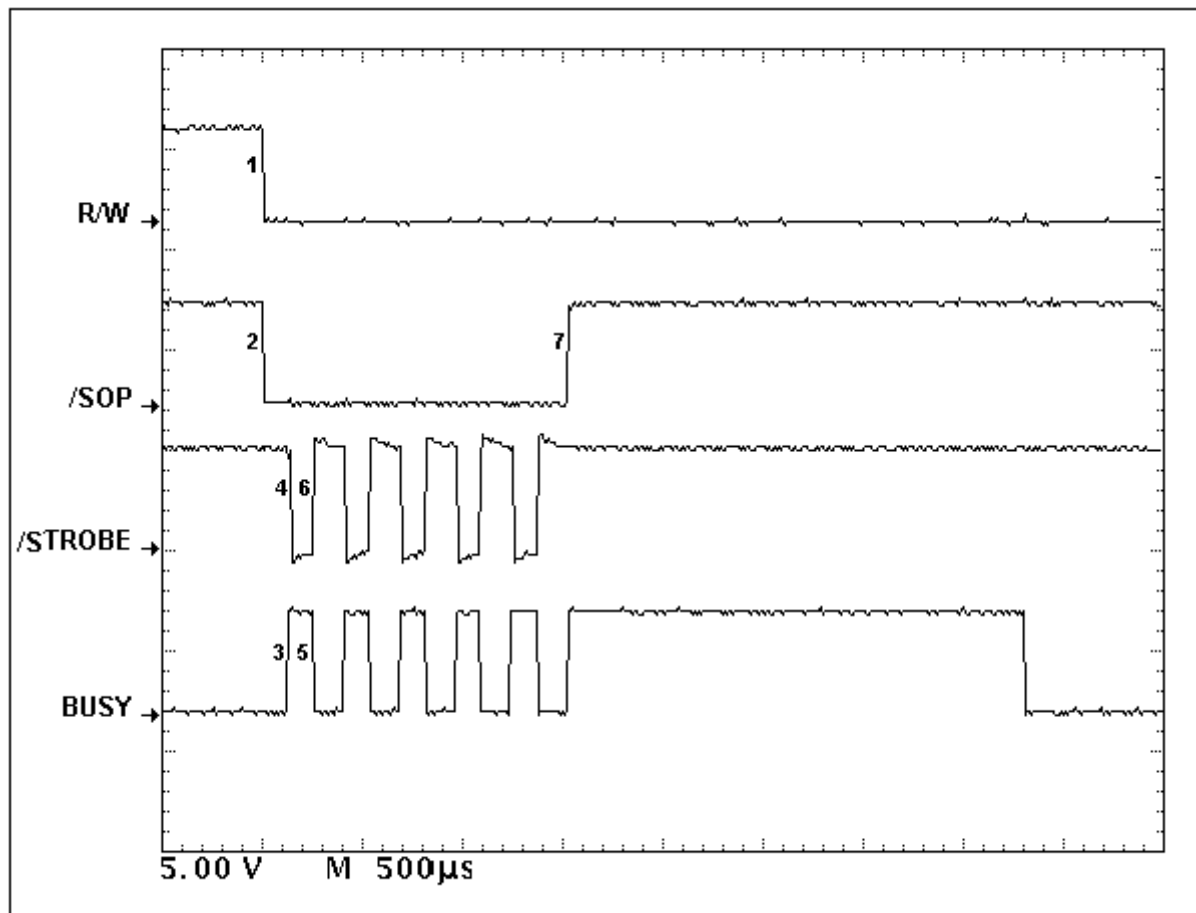
Figure 13: SKB enhanced mode 5-byte write (master to slave) – high-speed

The following actions correspond to numbered events in Figure 13:

1. The R/W line is pulled low to indicate write-to-SKB operation

2. The /SOP line is then asserted (low) to indicate the start of a command packet.

3. The BUSY line of the SKB switch is asserted (high) to indicate /SOP processing.

4. Binary data is written to the data lines (D0 to D7), and the /STROBE line is asserted (low) to indicate to the SKB switch that the byte can be read.

5. The BUSY line transitions to the idle (low) state to indicate that the SKB switch has read the byte.

6. The STROBE line is de-asserted (high), the SKB switch then asserts (high) BUSY to complete the byte transfer. All subsequent bytes are strobed-in to the SKB switch in the same way.

7. After BUSY transitions high following the final byte, the /SOP line is de-asserted (high) to indicate end-of-packet.
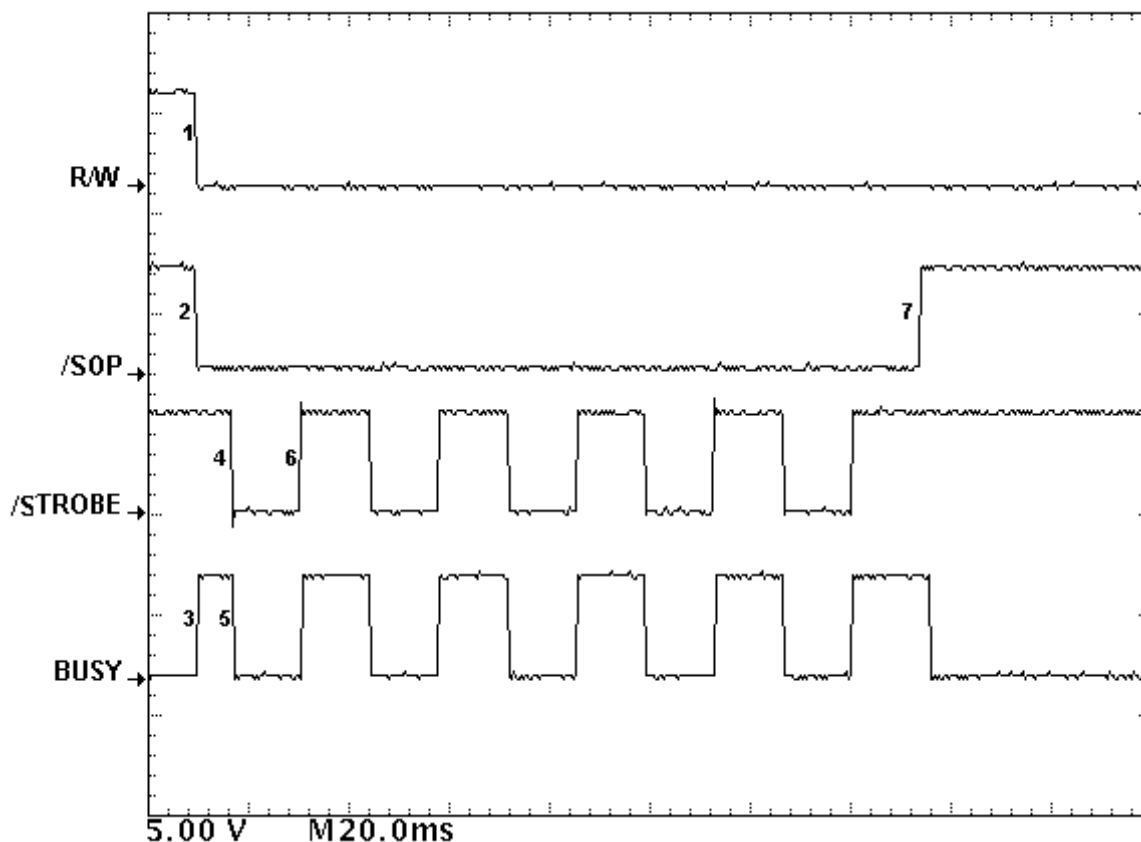
Figure 14: SKB enhanced mode 5-byte write (master to slave) – low-speed

Read Cycle

The read cycle refers to the bus master strobing bytes out of the SKB slave. In this mode, the master ensures that the R/W line is pulled high. The master then toggles the /SOP line from the high to the low state, which signals the SKB switch to place the first data byte on the data lines. The BUSY line is held high to indicate to the master that a valid byte has been placed on the data lines. The master reads the data lines and sets the /STROBE line to low to indicate that the read is complete. The SKB switch subsequently pulls the BUSY line low to signal that the data acknowledgment has been received. The master then sets the STROBE to high. The BUSY transitions to high to indicate to the master when the next byte has been placed on the data lines, and the process is repeated. Upon completion of the last data byte transmission, the master resets the /SOP line from the low to the high state to indicate the end of the data packet.

Figure 15 (high-speed master ~200 μs /STROBE pulse width) and Figure 16 (low-speed master -- ~18ms /STROBE pulse width) are oscilloscope trace captures showing typical line toggling for a master read cycle. These figures show the relationship between R/W, /SOP, and /STROBE input

lines and the BUSY output line during a three-byte response packet read from the SKB. Note that in each scenario illustrated, the line toggling is identical and independent of the /STROBE pulse time.


Figure 15: Three-byte response packet read from SKB – high speed

The following actions correspond to numbered events in Figure 15 and Figure 16:

1. The R/W line is driven high to indicate read-from-SKB operation.

2. The /SOP line is then asserted (low) to indicate the start of a command packet.

3. The BUSY line of the SKB switch is asserted (high) to indicate the first byte of the packet has been written to the data bus.

4. Binary data is read from the data lines (D0 to D7) and the /STROBE line is asserted (low) to indicate to the SKB switch that the byte was read.

5. The BUSY line is de-asserted (low) to indicate to the master that the SKB switch is ready to send another byte.

6. The /STROBE is de-asserted (high) to indicate to the SKB switch that the master is ready to accept another byte.

7. The BUSY is asserted (high) to indicate to the master that another byte has been written to the data bus. All subsequent bytes are processed in the same fashion to indicate the master has read the data bus.

8. The BUSY line is asserted (high) to indicate packet parsing and driven low when end-of-packet processing is complete.

9. The /SOP line is de-asserted (high) to indicate end of packet.

Figure 16: Three-byte response packet read from SKB – low speed

APPLICATION NOTE: RS-485 Packet Examples

The intent of this application note is to provide detailed information regarding RS-485 link layer packets and generating a CRC-16.

The SKB implements a differential-signal RS-485 network protocol which is capable of connecting 32 unit load devices (one bus master and up to 31 SKB slaves). The network layer of the RS-485 protocol is handled by transceivers connected to the UART of the SKB. Transmitting and receiving RS-485 differential data is transparent to the user. The remaining network protocol is largely implemented by sending and receiving data in RS-485 link-layer packets.

The purpose of link-layer packets is to provide a mechanism for getting command packets into a particular SKB device. Standard command packets are placed in the data payload section of the link-layer packet. Graphically, the RS-485 link packet is as follows:
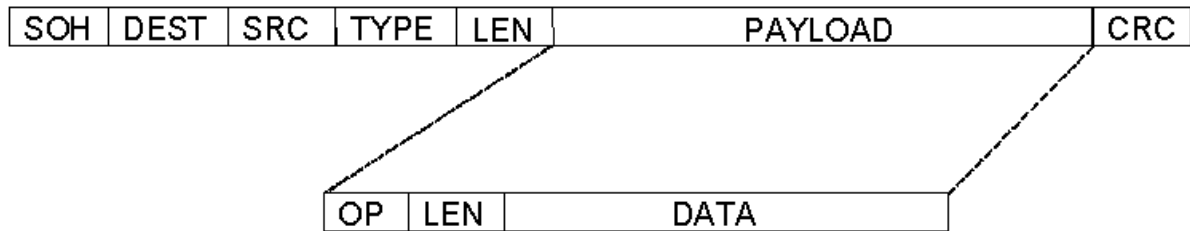
SOH	The START-OF-HEADER byte, always defined as 0x81. If a LEN, PAYLOAD, or CRC byte is has a value of 0x81, the byte should be actually transmitted twice. This indicates that the bytes should be interpreted as a valid packet byte rather than a SOH.	1 byte
DEST	The destination device address where the packet is being sent. All other devices will ignore the rest of the packet bytes.	1 byte
SRC	The device address of the sender. This byte is remembered and used to send ACK or response packets.	1 byte
TYPE	Defines the purpose of the packet: a value of 0 means this is a packet containing data, and a value of 1 means this packet is an ACKnowledgement to a previous data packet.	1 byte
LEN	The total number of payload data bytes (8-bits) . This number does **NOT** include the CRC bytes, which are concatenated to the end of the packet prior to actually transmitting.	2 bytes
PAYLOAD	These bytes represent the non-RS-485-specific data portion of the link-layer packet. Typically, a complete command (or response) packet is included in this field. The RS-485 sub-system will pass this payload up to the session/application layer of the software.	< 256 bytes
CRC	The cyclical redundancy check (CRC) is calculated on the assembled link-layer packet (including any/all byte swapping).	2 bytes

The RS-485 protocol is based on a command-acknowledge architecture: For each link-layer packet sent, an acknowledgement (in the form of and ACK packet) is provided.

RS485 Packet Example

Assume that a device with network address of 1 is present on the RS-485 network. The master will connect input channel 1 to output channel 2 on the first logical switch by sending the following command:

SWITCH 1 1 2

Translated into a command packet, the above command is represented as:

OPCODE	LENGTH	SWITCH	INPUT	OUTPUT
0x20	0x03	0x01	0x01	0x02

To transmit via RS-485 to device address 1, the following RS-485 link-layer packet is created. Note above command packet bytes in payload portion.

SOH	DEST	SRC	TYPE	LEN		PAYLOAD					CRC	
0x81	0x01	0x00	0x00	0x05	0x00	0x20	0x03	0x01	0x01	0x02	0x2a	0xf0

The master would expect the following acknowledge (ACK) packet to be sent back from device address 1. Note that the actual number of bytes returned is 4, other bytes (shown as n/a) are for illustrative purposes.

SOH	DEST	SRC	TYPE	LEN		PAYLOAD					CRC	
0x81	0x00	0x01	0x01	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

APPLICATION NOTE: CRC Examples

The intent of this application note is to provide detailed information regarding generation of CRC-16 for use with the RS-485 Serial and Enhanced Parallel interfaces.

CRC Generation

In the above example (App Note: RS485 Packet Example), the CRC-16 value 0xF02A is appended to the end of the link-layer packet prior to actually being transmitted by the master. Because the CRC is a 16-bit value, bytes are swapped (high byte-low byte) as per the standard command packet byte-order protocol described "Byte Order" on page 25.

Using the above example, the CRC-value was calculated using the assembled link-layer packet from the SOH byte (0x81) up-to and including the final PAYLOAD byte (0x02).

The following C-Code fragment illustrates an example of how the CRC is generated.

C-Code Generation of CRC Example

```
/**************************************************************************\
*                                                                         *
*                    (c) JDS Uniphase Corporation 2001                    *
*                         Nepean, Ontario, Canada                         *
*                                                                         *
***************************************************************************
*   FILE NAME:                                                            *
*                                                                         *
* DESCRIPTION: Win32 console app                                          *
*                                                                         *
*      NOTES:                                                             *
*                                                                         *
*    HISTORY: Date          Name        Revision                         *
*             ----          ----        --------                         *
*             May 2001      DP          Created for SKB testing.         *
\**************************************************************************/

#include <process.h>
#include <stdio.h>
#include <conio.h>




/***************************************************************************
 *    FUNCTION  : calc_crc16                                              *
 * DESCRIPTION  : Calculate CRC-16 value for RS-485 PACKET AND CRC EXAMPLE *
 *                application note link-layer packet example.             *
 *     INPUTS   : unsigned char *ptr - pointer to link layer packet.      *
 *                int count - number of bytes in packet                   *
 *     RETURNS  : int - CRC value. On WIN32 int is 32-bits - CRC appears in *
 *                the low-order 16 bits.                                  *
 *      SCOPE   : Global                                                  *
 ***************************************************************************
 *      NOTES  :                                                          *
 ***************************************************************************/
int calc_crc16(unsigned char *ptr, int count)
{
    int crc, i;

    /* Initialize crc to 0 for XMODEM, -1 for CCITT. */
    crc = 0;

    /* cycle through all bytes and add to CRC */
    while (--count >= 0)
    {
        /* XOR the running CRC value with next byte bit-shifted */
        crc = crc ^ (int)*ptr++ << 8;

        /* shift the CRC bits up or wrap with poly if 1 high bit set */
        for (i = 0; i < 8; ++i)
        {
            if (crc & 0x8000)
```

```c
                crc = crc << 1 ^ 0x1021;
            else
                crc = crc << 1;
        }
    }

    /* zero high-order 16 bits and return low-order 16-bit of the CRC */
    return (crc & 0xFFFF);
}


/****************************************************************************
 *     FUNCTION   : main                                                    *
 * DESCRIPTION    : Calculate CRC-16 value for RS-485 PACKET AND CRC EXAMPLE *
 *                  application note link-layer packet example.             *
 *       INPUTS   : none.                                                   *
 *      RETURNS   : none.                                                   *
 *        SCOPE   : Global                                                  *
 ****************************************************************************
 *        NOTES   : WIN32 int is 32-bits - CRC value appears in the low-order *
 *                  16 bits.                                                 *
 ****************************************************************************/
void main(void)
{
    unsigned char Packet[256];
    int crc;

    /* Build RS-485 Link layer packet as per example */

    Packet[0]  = 0x81;  /* SOH                 */
    Packet[1]  = 0x01;  /* DEST                */
    Packet[2]  = 0x00;  /* SRC                 */
    Packet[3]  = 0x00;  /* TYPE ( 0=DATA )     */
    Packet[4]  = 0x05;  /* LEN (low byte)      */
    Packet[5]  = 0x00;  /* LEN (high byte)     */
    Packet[6]  = 0x20;  /* PAYLOAD 1 (opcode) */
    Packet[7]  = 0x03;  /* PAYLOAD 2 (length) */
    Packet[8]  = 0x01;  /* PAYLOAD 3 (switch) */
    Packet[9]  = 0x01;  /* PAYLOAD 4 (input)  */
    Packet[10] = 0x02;  /* PAYLOAD 5 (output) */

    /* calculate the CRC */
    crc = calc_crc16( Packet, 11);

    /* output some stuff */
    printf("\n\nCRC-16 Calculation Utility");
    printf("\n\nCRC: %X", crc);
    printf("\n\nAny key exits...");

    /* get user input to exit */
    getch();

    /* exit in a sane fashion */
    exit(1);
```

APPLICATION NOTE: Implementation of the SKB in an existing SK/SP Application (using the Simplex Parallel Interface)

The intent of this application note is to describe the physical interface translation to allow an SKB switch to be backward-compatible with an SK controller. In this mode, the SKB switch is functionally compatible to an SK switch.

The pins allocated to SK emulation are located in the center portion of the 2x25 connector allowing direct ribbon cable drop-in to existing applications.

To connect an existing SK controller to a SKB II unit, an adapter cable assembly is required. The wiring information is contained in Table 12, below.

An illustration of an SKB device with an SK emulation cable is shown in Figure 17
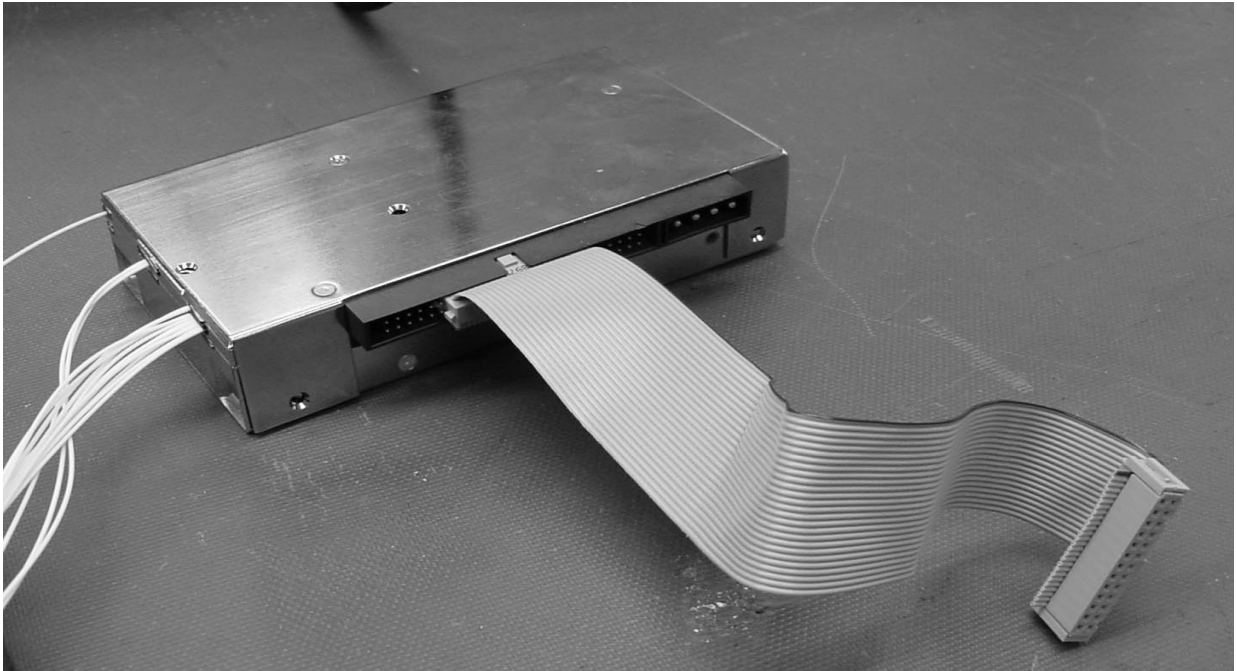

Figure 17: SKB with SK/SP Emulation Adaptor Harness

SK/SP to SKB Pinout comparison and Harness Wiring

Table 12: SKB II to SK Adapter Harness Wiring

SKB II PIN	SK PIN	SIGNAL	DESCRIPTION
13	1	GND	Ground
14	2	GND	Ground
15	3	BUSY	Busy output: low=idle, high= switching
16	4	D0	Data line 0
17	5	ERROR	Reset error output low = normal, high = switch mechanism position check failed (channel position is verified when SK switch is reset)
18	6	D1	Data line 1
19	7	GND	Shield
20	8	D2	Data line 2
21	9	GND	Shield
22	10	D3	Data line 3
23	11	GND	Shield
24	12	D4	Data line 4
POLARIZING KEY	POLARIZING KEY		
25	13	/STROBE	/STROBE input, active low = read data lines; high = ignore state of data lines. Note: The home line is also read in via the STROBE signal
26	14	D5	Data line 5
27	15	GND	Shield
28	16	D6	Data line 6
29	17	GND	Shield
30	18	/HOME	Home input: low sends the switch to the home position. Note: the state of the /Home line is only checked when the strobe line is active.
31	19	GND	Shield
32	20	GND	Ground
33	21	+5 VDC	+5 volt supply[1]
34	22	D7	Data line 7
35	23	+5 VDC	+5 volt supply[1]
36	24	+5 VDC	+5 volt supply[1]
37	25	NC	No connect
38	26	NC	No connect

Note: If powering SKB via the signal connector the cable length may not exceed 8 inches.

An adapter cable assembly is available from JDS Uniphase under part number ED0-A-00, as shown in Figure 18.
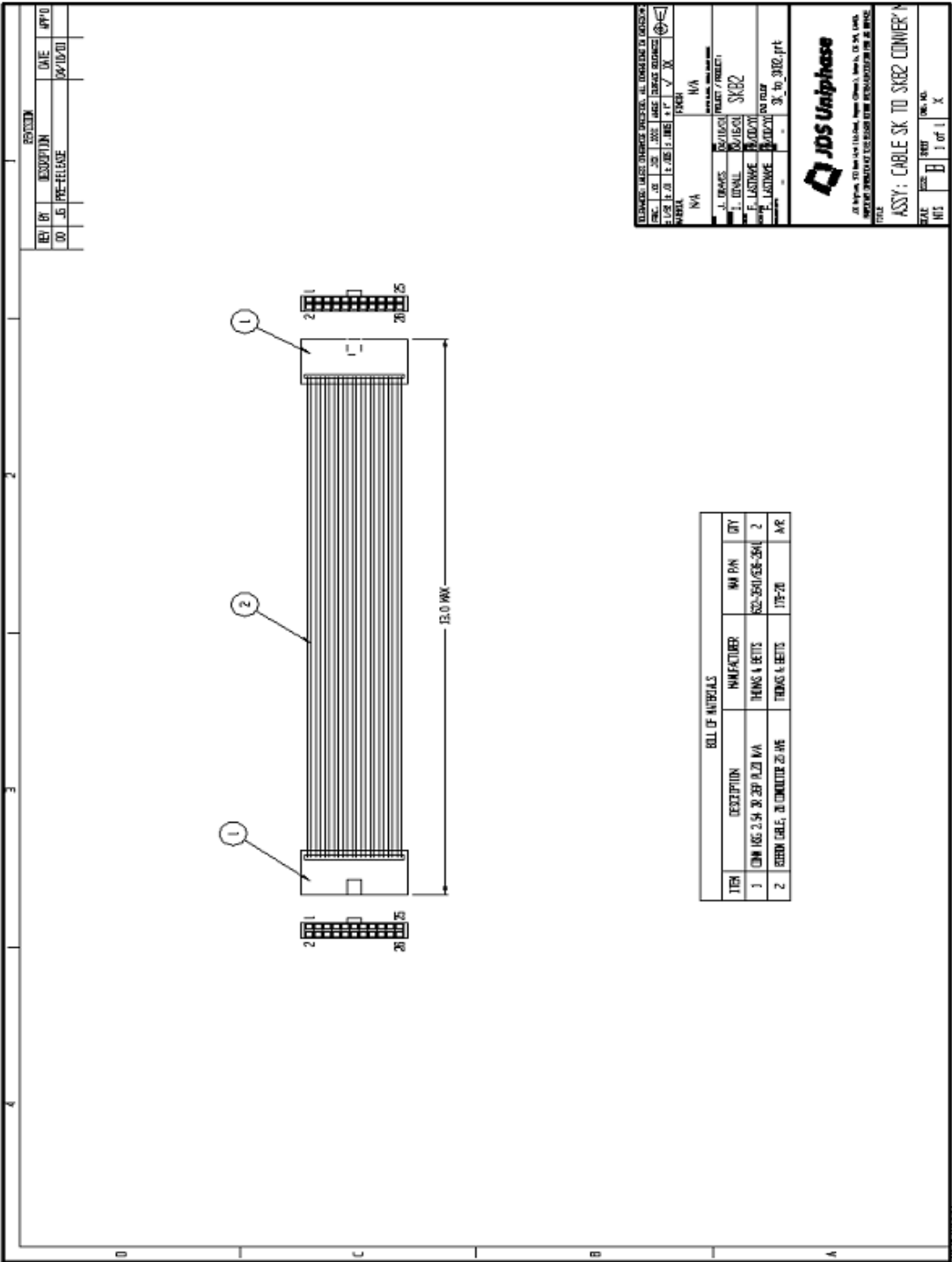

Figure 18: SKB to SK/SP Adapter Cable Assembly Drawing

APPLICATION NOTE: Controlling An SKB Switch using a PC Printer Port

The intent of this application note is to define the physical interface required to control an SKB switch via a standard PC enhanced parallel port (EPP).

Note that a graphical interface is available from JDS Uniphase Corp. for the purpose of evaluation of the SKB product.

Setting the Computer to EPP Mode

In order to interface with the SKB switch via the computer parallel port, it is necessary to make the data lines bi-directional, accomplished by using a parallel port operating in EPP mode.

To set the PC to EPP mode:

1. Use the PC operating manual and configure the parallel port for EPP, entering into the computers BIOS mode/setup and changing (or confirming) the port.

Using the Printer Port

To use the printer port with the switch:

1. Construct a cable wired as outlined inTable 13.

Table 13: Cable Wiring for Printer Port LPT2 Use

Printer Signal Name	Register Bit (Hex Address) Number	PC Connector Pin	SKB Pin	SKB Signal Name
Line Feed	(37A) 1[1]	14	20	/STROBE
Data 0	(378) 0	2	14	D0
Data 1	(378) 1	3	2	D1
Data 2	(378) 2	4	3	D2
Data 3	(378) 3	5	16	D3
Data 4	(378) 4	6	17	D4
Data 5	(378) 5	7	5	D5
Data 6	(378) 6	8	6	D6
Data 7	(378) 7	9	19	D7
PE	(379) 5	12	8	BUSY
STROBE	(37A) 0[1]	1	12	R/W
SLCT	(379) 4	13	9	ERROR
SLIN	(37A) 3[1]	17	22	/HOME
INIT	(37A) 2[1]	16	11	/SOP
Printer Port Ground[2]		18, 19, 20, 21, 22, 23, 24, 25	1, 4, 7, 10, 13, 15, 18, 21, 24	Shield[2]
			Power Source Ground	Power Ground

1.   Invert the signals on these lines.
2.   Connect these lines with the shield lines wrapped around the signal lines.

3. Connect the cable between the printer port and the parallel interface connector of the SKB switch.

4. Connect a 5 V power source to the power connector of the SKB switch

5. IMPoConnect a ground wire between the PC chassis and the power source ground.

APPLICATION NOTE: Custom SKB with D Subminiature Style connectors

A variant of the SKB has been developed that has a more ruggedized connector interface. That variant is described in this application note.

All control information contained in the body of this manual applies to this variant. Hence, this application note addresses physical features only.

Connector Description

Figure 19 shows the connector locations for the SKB switch. There are two connectors on the switch. The first connector is a 25-pin D-subminiature connector used by the parallel interface. The second connector is a 9-pin D-subminiature connector, which provides for the power connection and the RS485 Serial interface. A separate chassis ground connection point also is provided.
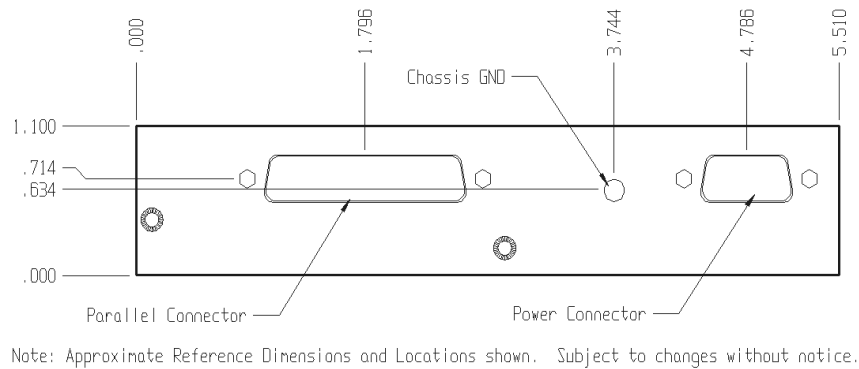

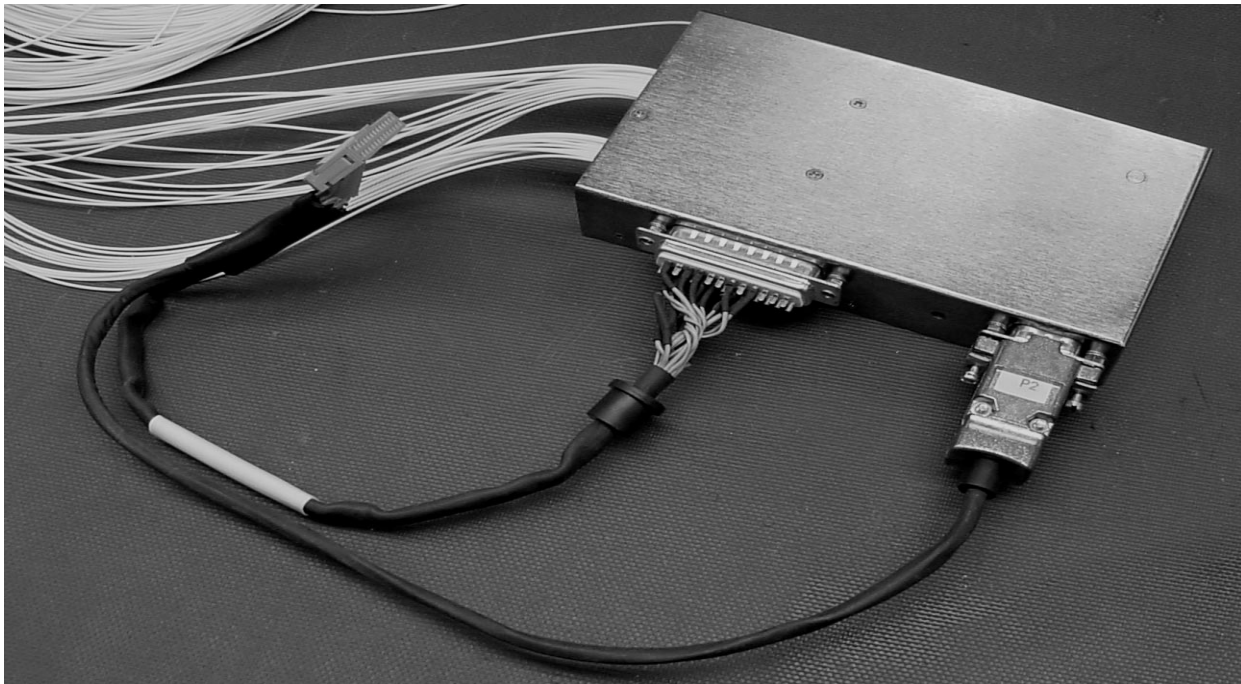**Figure 19: Connector and Port Locations**

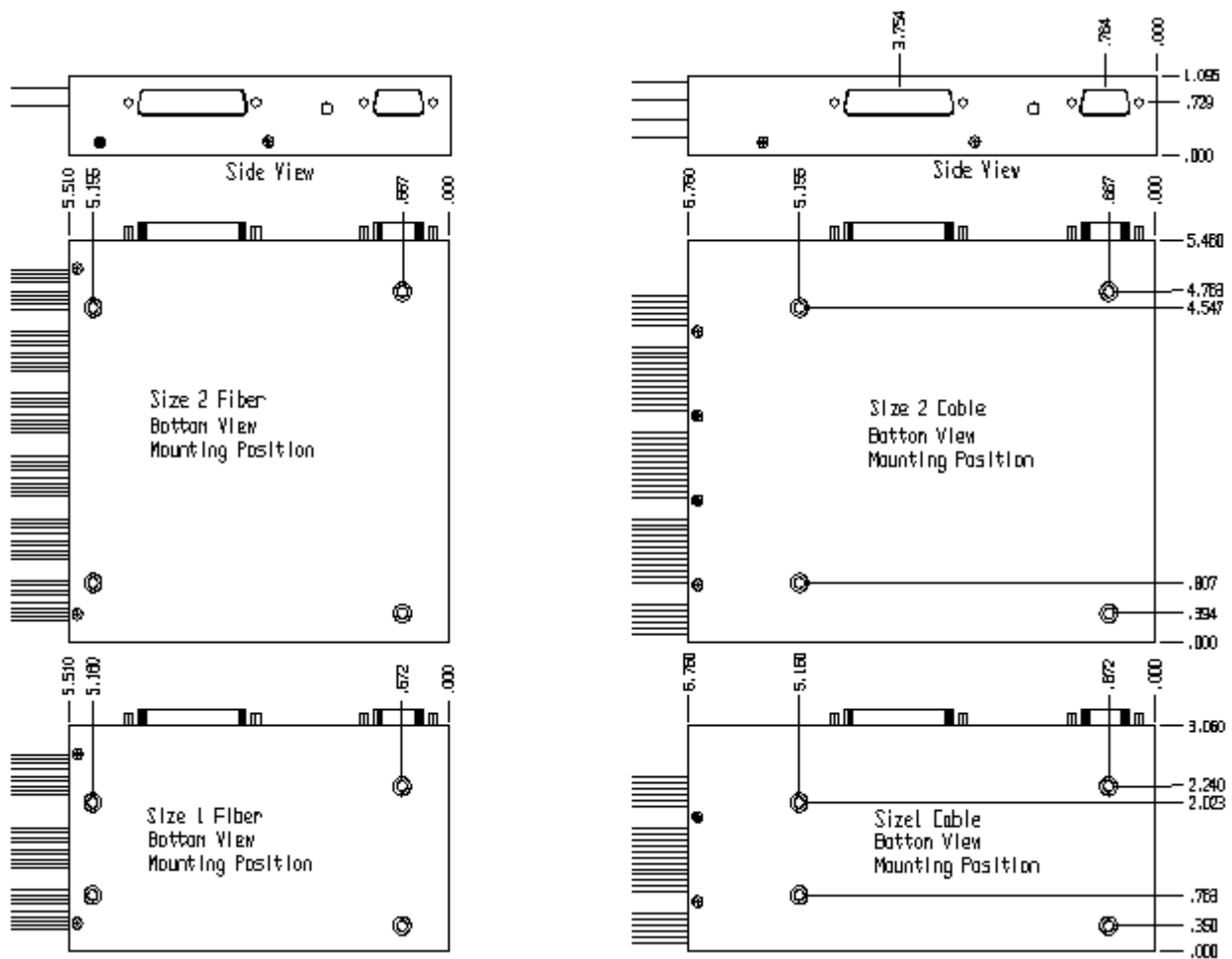**Figure 20: Connector and Port Locations**

Figure 21: Mounting Hole Location

The Power and Serial Interface Connector

The 9-pin D-subminiature connector is used for power and serial RS485 interface.

The signals for power and communication are connected via the D-subminiature 9-pin serial connector (Figure 23 and Table 14).
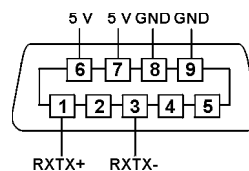

Figure 22: Pin Assignment

Table 14: Pin Assignment

Pin	Signal	Description	Functionality
Pin 1	RXTX+	Transmit/receive data positive side (B)	TXA. Differential input/output signal from the RS485 host.
Pin 2	Shield	Signal shield	This line is connected to chassis ground at the host end and is isolated at the slave. The two data lines are run as a twisted pair. The Power and Ground lines are run as twisted pair. The shield is used to encase both of the twisted pairs within the cable.
Pin 3	RXTX-	Transmit/receive data negative side (A)	TXB. Complement of the differential input/output from the RS485 interface.
Pin 4	Trigger	Active low trigger signal, transistor-to-transistor logic (TTL), multi-ended, pulled UP at slave with 100 K	This line is driven by the host processor (master) to indicate to the slaves that a trigger-based action is to be executed on the falling edge of this signal. This action is usually pre-conditioned by a request to the applicable slaves.
Pin 5	Attention	Active low attention signal, open collector, pulled UP at master with 470 ohm	This line is driven by the SKB module (slave) to indicate to the master that it requires the host attention. The master is expected to poll the slaves to determine which slave requires attention. This signal is an open collector signal that is terminated at the host end by a 470 ohm resistor connected to Vcc.
Pin 6	V+	5 V supplies in	5 V ±5% (1 to 2.5 A maximum, configuration dependent)
Pin 7	V+	5 V supplies in	5 V ±5% (1 to 2.5 A maximum, configuration dependent)
Pin 8	GND	Power ground	These lines are connected to the power supply ground, not to the chassis ground.
Pin 9	GND	Power ground	

The Parallel Interface

The 25-pin D-subminiature connector is used for the parallel interface.

The pin assignment for the parallel interface is outlined in Figure 23 and Table 15.
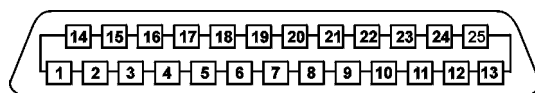

Figure 23: Pin Assignment

Table 15: Pin Assignment

Pin	Signal	Description
1	GND	Shield
2	D1	Data line 1
3	D2	Data line 2
4	GND	Shield
5	D5	Data line 5
6	D6	Data line 6
7	GND	Shield
8	BUSY	Busy output: low = idle high = operation in progress (switching)
9	ERROR	Error output: low = normal high = error in error queue
10	GND	Shield
11	/SOP	Start of packet--provides a start-and-stop mechanism
12	R/W	Read/write--driven by master read and write cycles
13	GND	Shield
14	D0	Data line 0 input; least significant bit (LSB)
15	GND	Shield
16	D3	Data line 3
17	D4	Data line 4
18	GND	Shield
19	D7	Data line 7; most significant bit (MSB)
20	STROBE	STROBE input, active low: high-to-low pulse = read data lines and home line high = ignore state of data lines and home line This line is internally pulled high via 10 K ohm resistor to 5 V DC
21	GND	Shield
22	RESERVED	Reserved; internal use only; do not use
23	RESERVED	Reserved; internal use only; do not use
24	GND	Shield
25	RESET	Resets the hardware (MCU reset)

Service

Immediately inform JDS Uniphase and, if necessary, the carrier, if

- The contents of the shipment are incomplete.
- The unit or any of its components are damaged or defective.
- The unit does not pass the initial inspection.

In the event of carrier responsibility, JDS Uniphase will allow for the repair or replacement of the unit while a claim against the carrier is being processed.

Returning a Unit

Repairs must be done by qualified personnel.

Avoid returning a unit that is functioning properly. Read this section thoroughly before returning a unit.

JDS Uniphase only accepts returns for which a Return Material Authorization (RMA) has been issued.

Perform the following steps to obtain an RMA:

1. Contact JDS Uniphase sales personnel or an RMA Servicing representative to obtain an RMA form and number. The following information is required:

    - Model number and serial number of the unit
    - Detailed description of the defects or problems
    - Owner's name, address, and contact phone number
    - Date of purchase

Shipping a Unit

Perform the following steps to ship the unit:

1. Wear an anti-static wrist strap and work in an ESD-controlled area.

2. Pack the unit in the original shipping container and packing material.

3. When these materials are unavailable, the following guidelines are suggested:

    a. Cover the front panel with a strip of cardboard.
    b. Wrap the unit in anti-static packaging. Use anti-static connector covers.
    c. Pack the unit in a reliable shipping container.
    d. Use enough shock-absorbing material (10 to 15 cm on all sides) to cushion the unit and to prevent it from moving inside the container. Pink poly anti-static foam is the best material.

4. Seal the shipping container, and clearly mark FRAGILE on its surface.

5. Mark the RMA number on the shipping container.

6. Ship the unit to the address given in the Getting Help section on page iii.

    Note: Shipping, brokerage, and duty charges are the responsibility of the customer.